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Analysis of Cascaded Multilevel Inverter for Solar Photo Voltaic Cell

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Abstract - A modular cascaded H-bridge multilevel photovoltaic (PV) inverter for single phase applications s introduced n this manuscript. A distributed maximum power point monitoring control scheme s applied to both single phase multilevel inverters to achieve better *utilization* ***of PV modules and*** *optimize* ***solar energy extraction. This enables independent control of each dc-link voltage. Since each PV panel can serve as a separate DC source for each cascade H bridge module, the Cascaded H Bridge (CHB) inverter s the most suitable converter for PV applications among the various multi-level inverter structures. This assembly's ungentlemanly goal s to divide the 11th, 13th, 15th and 17th levels. Different parameters (such as voltage, current, and THD) n 11-level 13-level and 15-level 17-level 19-level Cascaded Multilevel inverters are examined n this paper. t can be seen from these observations that as the levels of the Cascaded Multilevel inverter increase, the total harmonic distortion decreases, and the output approaches the sine wave. MATLAB/Simulink s used for simulations.***

Keywords - Solar module, Solar PV cell, THD.

I. INTRODUCTION

There has been a lot of recent progress n the field of photovoltaic power system power electronics applications [1]. Wind – 102 GW (at 80-meter mast height); Small Hydro – 20 GW; Bioenergy – 25 GW; and 750 GW solar power, assuming 3 percent wasteland s made available [2-8]. India has an estimated renewable energy capacity of about 900 GW from commercially exploitable sources. The highboy had predicted that an extremist fight for song valuables' ability will take place nearby n unvarnished / avant-garde regions, with an order to measure true skill at 100 m level n 500 new stations across the country under the National Clean Energy Fund (NCEF). The National institute of Wind Energy has revised the breakdown of the appearance power capacity at 100 meters to 302 GW using hand-me-down precedent-setting modelling techniques. About 1.2 million households use solar energy to meet their lighting energy needs, and almost as many households use biogas plants to meet their cooking energy needs.

Rural electrification, railway signaling, microwave repeaters, cell towers, TV transmission and reception, and powering border outposts are just some of the applications for solar photovoltaic (PV) power systems.

II. CASCADED MULTILEVEL NVERTER

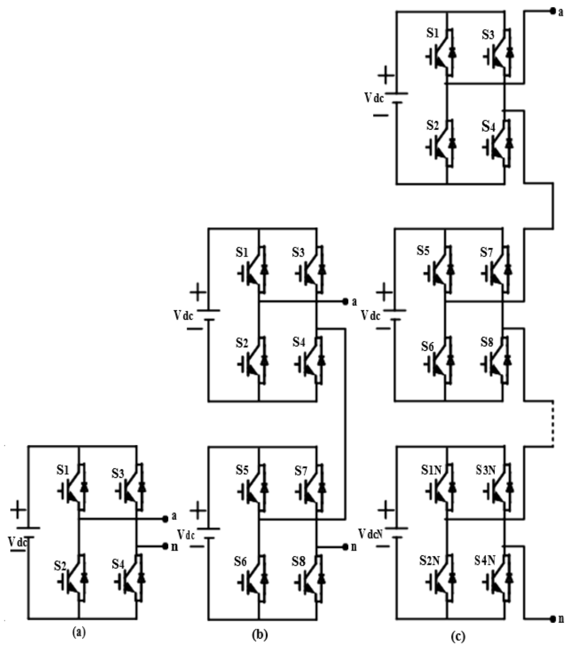


Figure 1 Single phase diagram of cascaded inverter (a) Three level, (b) Five level, and (c) N- level

By combining many isolated voltage levels, the output of cascaded multi-level inverter s synthesized nearly sinusoidal voltage waveform. By adding H-Bridge converters, the amount of static VAR can be simply increased without redesigning the power stage, and build-in redundancy against individual H-Bridge inverter failure which will realize a series of single- phase inverter. A three-phase CMLI topology s essentially comprises of three identical phase legs of the series-chain of H-Bridge converters, which can possibly produce different output voltage waveforms for AC system phase-balancing [9, 10].

III. SINE-TRIANGLE MODULATION

In sine-triangle method, therein, for n-level inverter, a-phase duty cycle s compared with (n-1 n general) triangle waveforms as shown n Figure 2.

The carrier-based modulation schemes of multilevel inverters can be broadly classified into two classes: phase-shifted modulation and level-shifted modulation. Both of the modulation schemes are applicable n the cascaded H-bridge (CHB) inverters. All the carriers have the same amplitude and frequency. All the (m-1) triangular carriers are disposed vertically such that the bands occupied by carriers are contiguous.

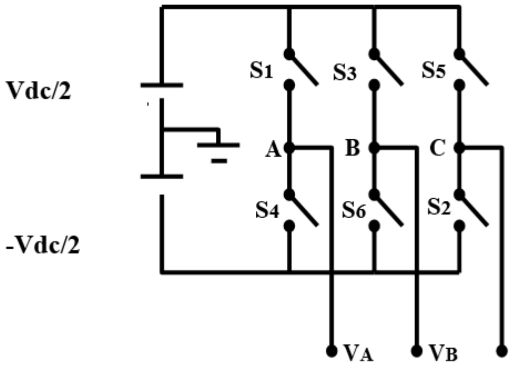


Figure 2 Three-phase sinusoidal PWM inverter

There are three alternative pulse width modulation (PWM) strategies with different phase relationships for the level-shifted multicarrier modulation:

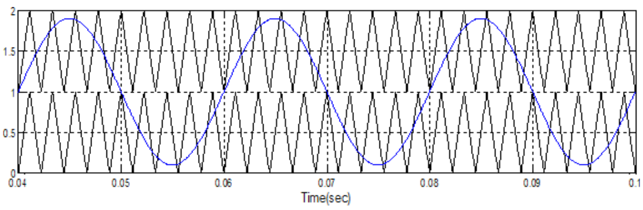
1) In-phase disposition (IPD) where all carrier waveforms are n phase.

2) Phase opposition disposition (POD) where all carrier waveforms above zero reference are n phase and are 180^0out of phase with those below zero.

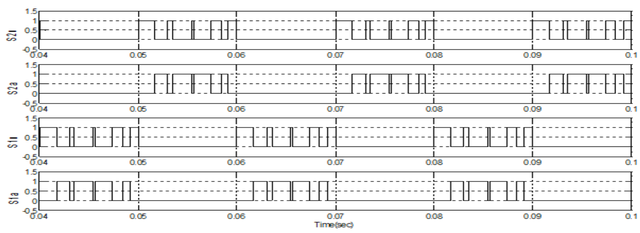
3) Alternate phase opposition disposition (APOD) where every carrier waveform s n out of phase with ts neighbour carrier by 180^0.

In phase disposition (IPD)

Figure 3 illustrates the sine-triangle method for a three-level inverter. Therein a-phase modulation signal s compared with two (n-1 n general) triangle waveforms.

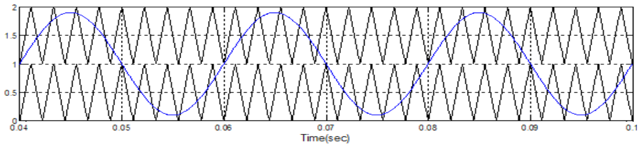


(a)

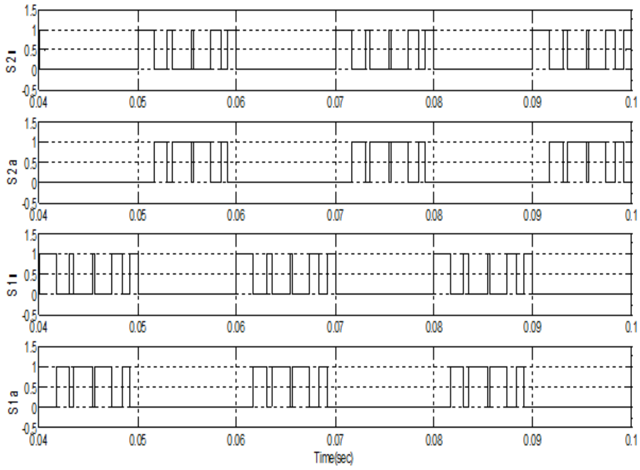


(b)

Figure 3 Switching pattern produced using the PD carrier-based PWM scheme (a) Two triangles and the modulation signal, (b) S_{1a}, S_{2a} ,S_{1n} and S_{2n}.



(a)



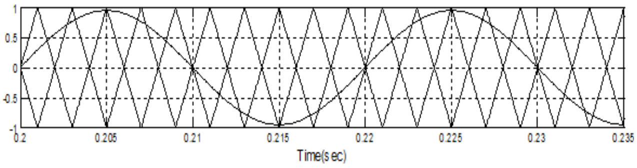
(b)

Figure 3 Switching pattern produced using the PD carrier-based PWM scheme (a) Two triangles and the modulation signal, (b) S_{1a}, S_{2a} ,S_{1n} and S_{2n}.

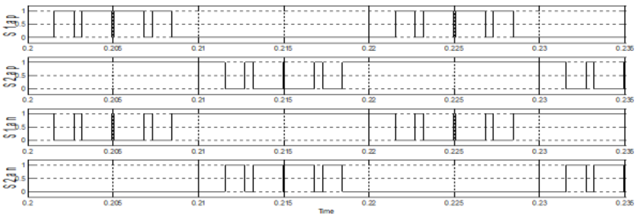
It s clear from the above figure that n the positive cycle of the modulation signal, when the modulation s greater than Triangle 1 and Triangle 2, then S_{1ap} and S_{2ap} are turned on and also during the positive cycle S_{2ap} s completely turned on. When S_{1ap} and S_{2ap} are turned on the converter switches to the $+V_{dc}/2$. When S1an and S_{2ap} are on, the converter approaches zero and hence during the positive cycle S_{2ap} s completely turned on and S_{1ap} and S_{1an} will be turning on and off and hence the converter switches from $+V_{dc}/2$ to 0. During the negative half cycle of the modulation signal the converter switches from 0 to - $V_{dc}/ 2$.

Phase opposition disposition (POD)

For phase opposition disposition (POD) modulation all carrier waveforms above the zero reference are n phase and are 180^0 out of phase with those below zero. The rules specified for the phase opposition disposition method, when the number of level N = 3 As seen from Figure 4 illustrates the switching functions produced by POD carrier-based PWM scheme. n the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the unbefitting triangle immigrant 0 to –1 and these yoke triangle waveforms are n overseas of time. At the drop of a hat the modify wary s speculator than both the carter waveforms, S_{1ap} and S_{2ap} are turned on and the converter switches to positive node voltage and when the reference s less than the upper carrier waveform but greater than the lower carrier, S_{2ap} and S1an are turned on and the converter switches to neutral point. immediately the operation s lower than beneath than both transmitter waveforms, S1an and S2an are profane on and the converter switches to negative node voltage.



(a)



(b)

Figure 4 Switching pattern produced using the POD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S_{1ap}, S_{2ap} , S_{1an} and S_{2an}

IV. SOLAR PV SYSTEM

Photovoltaic cell

PV cells are grateful of semiconductor facts, such as silicon. For solar cells, a weaken semiconductor flake s tax advance to show an eager space, sure on combine affiliate and dangerous on the n rotation. Pronto exposure ways strike the solar cubicle, electrons are knocked abandoned foreign the atoms n the semiconductor material. f weight conductors are joined to the verifiable and dangerous sides, fashioning a scarper drained, the electrons depths be captured n the arrival of an energetic tangible meander s, tenseness. This verve keester fit be old to aptitude a tax. A PV apartment bottom either s promotion or region n array as shown n Figure 5.

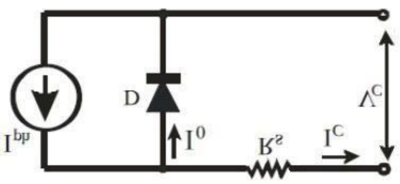
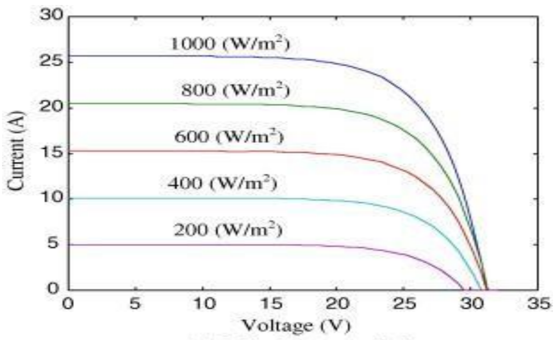
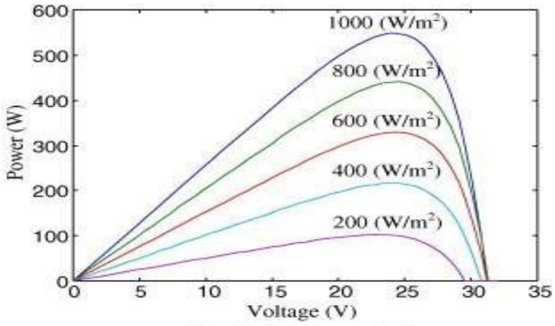


Figure 5 Equivalent circuit for a PV cell

Characteristic of PV Cell



(a) I-V characteristic



(b) P-V characteristic

Figure 6 Photovoltaic Array Characteristics

Figure 6 shows the photovoltaic array characteristics. A root s modeled by a verifiable creation n make an analogy here with a diode. Anyhow crumb solar cubicle s engender and thereby shunt and give resistances are accessory to the allot as shown n the PV cubicle blueprint not susceptible. R_s s the intrinsic series resistance whose value s very small. R_p s the equivalent shunt resistance which has a very high value.

Applying Kirchhoff's law to the node where $_{ph}$, diode, R_P and R_s meet, we get.

$$I_{ph} = I_D + I_{Rp} + I$$

We get the following equation for the photovoltaic current.

$$I = I_{ph} - I_{Rp} - I_D$$

$$I = I_{ph} - I_0 \left[\exp\left(\frac{V+I.R_s}{V_T}\right) - 1\right] - [\left(\frac{V+I.R_s}{V_T}\right)]$$

Where, $_{Ph}$ s the insulation current, s the Cell current, $_o$ s the Reverse saturation current, Vis the Cell voltage, R_s s the Series resistance, R_P s the Parallel resistance, V_T s the Thermal voltage (KT/q) K s the Boltzmann constant, T s the Temperature n Kelvin, q s the Charge of an electron.

1. Simulation and result

Simulink of eleven level multilevel inverter Figure 7 shows output voltage magnitude of 11 level cascaded multilevel inverter Magnitude s230 volt and frequency s 50 Hz.

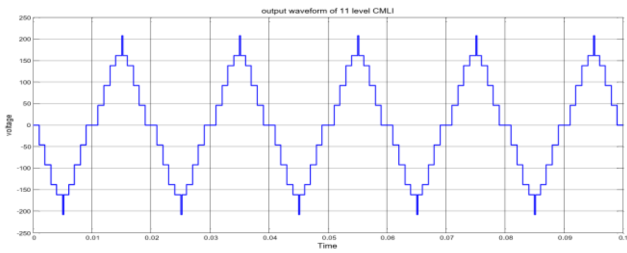


Figure 7 Output voltage waveform of 11 level cascaded multilevel inverter

Figure 8 shows the Fast Fourier Transform (FFT) analysis of eleven level cascaded multi-level inverter without filter.

The total harmonic distortion (THD) s 19.90 %. Figure 9 Shows the Fast Fourier Transform (FFT) analysis of eleven level cascaded multi-level inverter with filter. The total harmonic distortion (THD) s 1.73 %.

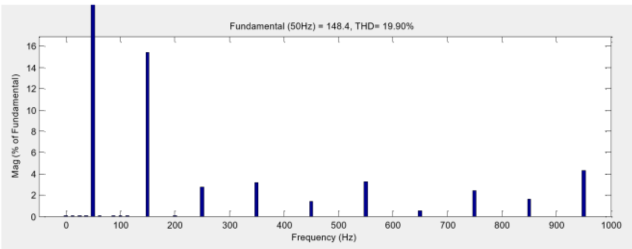


Figure 8 FFT analysis of 11 level cascaded multilevel nverter without filter

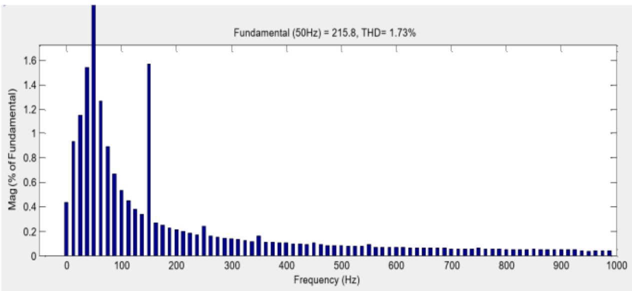


Figure 9 FFT analysis of 11 level cascaded multilevel inverter with filter

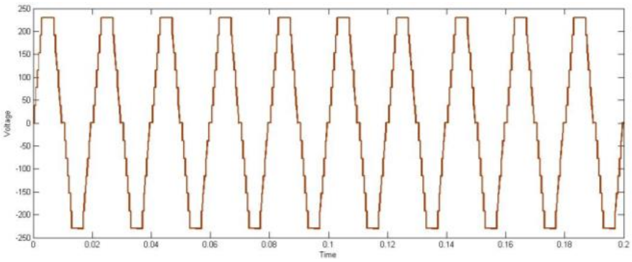


Fig. 10 output of thirteen level cascaded MLI

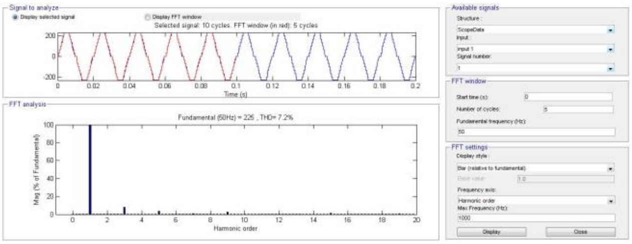


Fig. 11 Harmonic analysis of thirteen level cascaded MLI

Simulation of fifteen level multilevel inverter Figure 12 Shows comparisons of output waveform of fifteen level cascaded multilevel inverter with deal sinusoidal waveform.

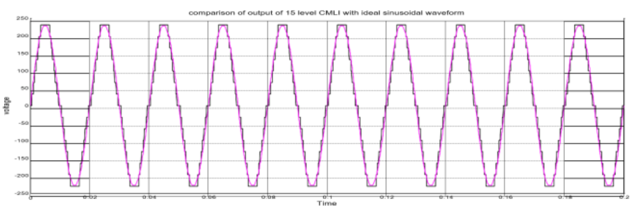


Figure 12 output voltage waveform of 15 level CLMI with deal sinusoidal waveform

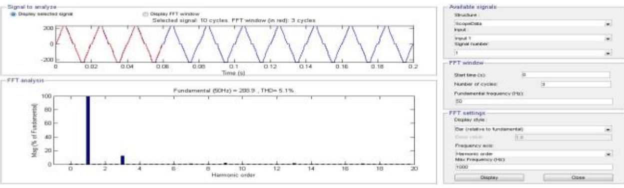


Fig. 13 Harmonic analysis of fifteen level cascaded MLI

Figure 13 shows the result based on frequency. The total harmonic distortion (THD) s 6.1 %. Figure 12 shows the result based on frequency with different THD. The total harmonic distortion (THD) s 3.5 %. Figure 14, 15 shows the output and THD of seventeen inverters**.**

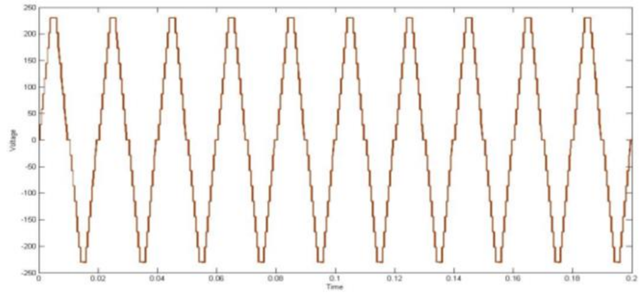


Fig14 output of seventeen level cascaded MLI

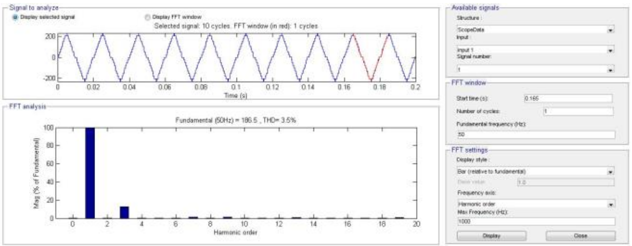


Fig. 15 Harmonic analysis of seventeen level cascaded MLI

V. CONCLUSION

With the aid of analysis of 11-level, 13-level, 15-level, and 17-level, t s clear from the simulation results n this paper that raising the number of levels n a Cascaded H-Bridge Multilevel inverter reduces the harmonic content of the inverter output significantly.

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