

Comparison of Transistor Clamped H-bridge and Cascaded Multilevel Inverter

Nisha Parveen¹, Rishabh Shukla²

¹Research Scholar, ²Prof.,

Deptt. Of Electrical and Electronics Engg., Oriental College of Technology, Bhopal

Abstract — Multilevel converters are appropriate for medium and high power applications as a result of its trait of synthesizing a sinusoidal voltage on few DC levels. They give great quality output resulting with lower harmonic distortion in the output and lower commutation losses. The primary impediment is their intricate circuit designs, requiring an incredible number of power devices and passive components, and a complex control circuitry. A new topology of multilevel inverter for 5-level utilizing the Conventional H-Bridge is proposed in this paper. The proposed topology is referred as new TCHB has the feature like boost output voltage capability along with capacitor voltage balancing. The proposed multilevel inverter uses four auxiliary switches and transistor clamped H-bridge (TCHB) with an bidirectional switch. The single cell of conventional H-bridge produces three-level output voltage similar to input DC voltage but the single cell of proposed topology produces five-level output with output voltage double the input DC voltage. The proposed new TCHB and old TCHB 5-level inverter are modeled and simulated on matlab / simulink and compared in terms of the output voltage, total harmonic distortion (THD), No. of switching devices used etc. From the results the proposed inverter provides more output voltage with less harmonics in the output voltage.

Keywords— multilevel inverter; conventional h-bridge; transistor clamped h-bridge; cascaded h-bridge; multicarrier pulse width modulation; transistor clamped inverter, cascaded neutral –point clamped inverter.

I. INTRODUCTION

Multilevel Inverters nowadays are widely accepted for medium and high power applications where AC to DC conversion is required [1]. The reason behind is that multilevel inverter topology produces staircase like output voltage waveform as the number of voltage levels increases, the harmonic content of the output voltage waveform decreases and it resembles the sinusoidal shape closely. The synthesized multilevel outputs are superior in quality which results in reduced filter requirements [2]. The multilevel topology offers reduced dv/dt across switches, switching losses constraint, high voltage and high power capabilities to avoid series-parallel connections of devices, improved power quality at supply side and load side, reduced THD level for same power level. The main theme for the development of multilevel inverter is reduction of power ratings of power devices and to reduce the cost by reduction in the device count, which can be

achieved by using various multilevel topologies. The inverters with three level or more than three-level in its output voltage are known as the multilevel inverters. Multilevel inverters are capable of producing high power high voltage as the unique structure of the multilevel voltage source inverter allows too get high voltages with low harmonics without the use of transformers or series connected synchronized switching devices. There are three major multilevel voltage source inverter topologies neutral-point clamped inverter (i.e. diode clamped), flying capacitor (capacitor-clamped) and cascaded H-bridge multilevel inverter. There are also various other topologies which have been proposed and have successfully adopted in various industrial applications. For the same number of power devices, H-bridge multilevel topologies [2]-[3] significant increase the level number of output voltage waveform. And therefore, these topologies become one of the most attractive approaches. One of the research topics is to increase the level number for the H-bridge multilevel topologies, such that the harmonic contents can be reduced as much as possible while keeping low switching frequency and switching losses. This paper mainly focuses mainly on the 5-level multilevel inverter based on H-bridge. Being the most reliable out of three topologies the cascaded multilevel inverter has the best fault tolerance owing to its modularity a feature that enables the inverter to continue operate at lower power levels after cells failure[4]-[6]. Due to the modularity of the cascaded multilevel inverter it can be stacked easily for high power and high voltage applications. The cascaded multilevel inverter mainly consists of several identical H-bridge cells which are cascaded in series from the output side. The H-bridge which are cascaded as per the requirement consists of DC source in each of its cells on the basis it (CHB) may further be classified as symmetrical if the input DC voltage is equal in all the cascaded power cells and as asymmetrical if the input DC voltage is not same for each power cell. The symmetrical CHB is more advantageous over the asymmetrical CHB in terms of modularity, maintenance and cost. In case of the asymmetrical CHB input DC voltage is varied in each power as per the requirement to increase the voltage levels [2], [3]. In case of the symmetrical CHB the voltage level can be increased

without varying the DC voltage with same number of power cells. The transistor clamped topology is popular now a days as it provides provision to increase the output levels by taking different voltage levels from the series stacked capacitors [7]-[8]. In this paper a new configuration of the transistor clamped H-Bridge based 5-level multilevel inverter is proposed which produces a five-level output voltage just like the old TCHB, but this new proposed topology produces the boost output voltage. Two different types of 5-level multilevel inverter

based on transistor clamped H-bridge are modeled. Also various topologies of multilevel inverter for 5-level are compared in terms of THD, switch count, output voltage magnitude.

II. CONFIGURATION OF PROPOSED TCHB 5-LEVEL INVERTER

The general block diagram for the proposed inverter is shown in fig.1 and the complete configuration of the proposed TCHB 5-level inverter topology is shown in fig.2 which is like the old TCHB with some modifications. Like the old TCHB the new proposed TCHB also consist of total of four main controlled switches forming conventional H-Bridge. Fig.3 shows the circuit diagram of the old TCHB. The new TCHB in extra consists of four auxillary switches Both the type of TCHB also consists of bidirectional switch, the old TCHB consists of Diode bridge with a single IGBT as an bidirectional switch where as new proposed TCHB consists of two anti paralleled NPT-IGBT's consisting of T11 and T12 in a single cell which is connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels (+2V_{dc}, +V_{dc}, 0, -V_{dc}, -2V_{dc}) based on the switching combination . The switches T1, T2, T3, T4 forms the H-bridge and the remaining switches A1, A2, A3, A4 are auxillary switches connected in the same leg which plays a role in boosting the voltage and the input DC voltage is connected with positive terminal between the switches A1 and A2 and the negative terminal between the switches A3 and A4. The capacitor voltage divider is formed by C1 and C2. The conventional H-bridge cascaded inverter consists of two cells and each cell consisting of equal DC voltage sources for each H-bridge and only four switching devices.

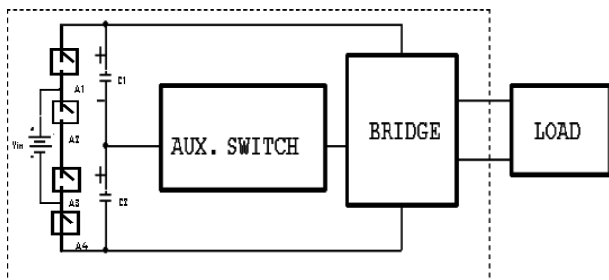


Fig.1 General block diagram of new topology

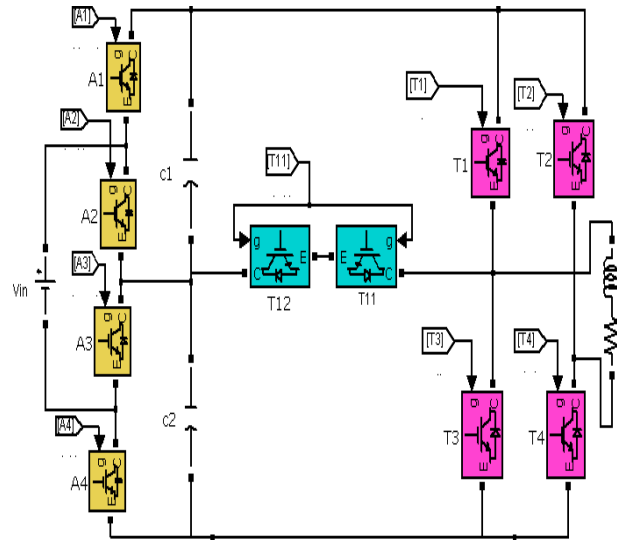


Fig.2 Proposed TCHB Single-phase 5-level multilevel inverter

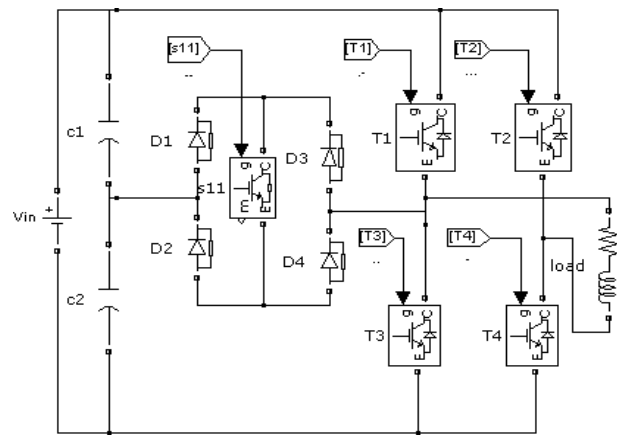


Fig.3 Single phase 5-level Transistor Clamped H-bridge inverter

III. COMPARISON OF DIFFERENT 5-LEVEL INVERTERS

Table.1 COMPARISON OF DIFFERENT 5-LEVEL INVERTER TOPOLOGIES

Multilevel Inverter	No. of Conducting switches	No. of auxillary switches	No. of Capacitor	No. of Diodes
Proposed TCHB	8	2	2	8
Old TCHB	4	1	2	8
Conventional H-Bridge	8	0	0	8
Diode Clamped	8	0	4	20
Capacitor Clamped	8	0	10	8

The number of conducting switch used in new TCHB are twice of that used in old TCHB and same as that used in

the cascaded conventional H-Bridge, diode clamped and capacitor clamped but for the same output voltage. The rating of the switches used in the new TCHB will be half of the rating of switches in old TCHB. The rating of the voltage source required for same output voltage will be half in comparison with the old TCHB and where as two separate voltage sources will be needed in case of CHB cascaded inverter. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches. Auxiliary devices (diodes and capacitors): just like the old TCHB the new proposed TCHB reduces the number of diodes by 60% (eight instead of 20) and the number of capacitors by 50% (two instead of four) when compared with the diode clamped configuration. The new configuration reduces the number of capacitors by 80% (two instead of 10) when compared with the capacitor clamped configuration.

IV. WORKING OF PROPOSED TCHB 5-LEVEL INVERTER TOPOLOGY

The working of the new TCHB based five-level inverter topology is explained telling how the required five level output is produced as:

1. Maximum positive output that can be produced is the double of the input DC voltage i.e $2V_{dc}$ which is produced when S21 is on connecting the load positive terminal to the load and S51 is on connecting the load negative terminal to the V_{dc} thus the total output voltage is $2V_{dc}$. The output voltage level V_{dc} is obtained when Sa1, S11, S51 and Sa2 gets turned on other switches remaining off.
2. Maximum negative output is $-2V_{dc}$ which is produced when switches S41 and S31 gets turned on connecting the negative and positive terminal of the load respectively to the input source. The negative level $-V_{dc}$ is obtained when switches Sa1, Sa3, S11, S41 are turned on other switches remaining off.

The detailed operation of the proposed topology can also be understand through the look up table which is given in Table 2. In the look up table 0 and 1 values are assigned to the switches for a particular voltage level. At any level of the output voltage the switches which are having value 1 means they are in the ON state at that time and the remaining switches with the zero value are in the OFF state at the same instant of time. The look up table for the proposed inverter is given in the figure given below.

Table.2 SWITCHING PATTERN FOR THE PROPOSED 5-LEVEL INVERTER

Voltage level	+2Vdc	+Vdc	0	-Vdc	-2Vdc
A1	0	0	0	1	0

A2	0	1	0	0	0
A3	0	0	0	1	0
A4	0	1	0	0	0
T11	0	1	0	1	0
T1	1	0	1	0	0
T2	0	0	0	0	1
T3	0	0	1	1	1
T4	1	1	0	0	0

V. PWM CONTROL SCHEME FOR NEW TCHB 5-LEVEL INVERTER

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage [1]. There are variety of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. This PWM is further divided into various PWM techniques such as single pulse PWM, space vector PWM, multiple pulse PWM, phase displacement control [1]. For this proposed topology we are using the multicarrier based control technique which can be applied to all the topologies of the multilevel inverter. For any given number of levels in the output voltage the number of carrier to be used is given as $N-1$ Where N is the number of levels in the output voltage. Fig.4 represents the triangular shape carrier waveform and the sinusoidal reference signal showing the pulse width modulation technique used for the control. Simply a reference signal is taken which is a sinusoidal signal of 50Hz frequency and this reference is compared with the carrier signal which are the triangular wave. The modulation index we are using in this modulation technique is 0.90. The advantage of this scheme is that it offers the charge balance control in the input DC sources and voltage across the capacitor are also balanced [12]. Fig.5 shows the simple circuit for the sinusoidal pulse width modulation scheme.

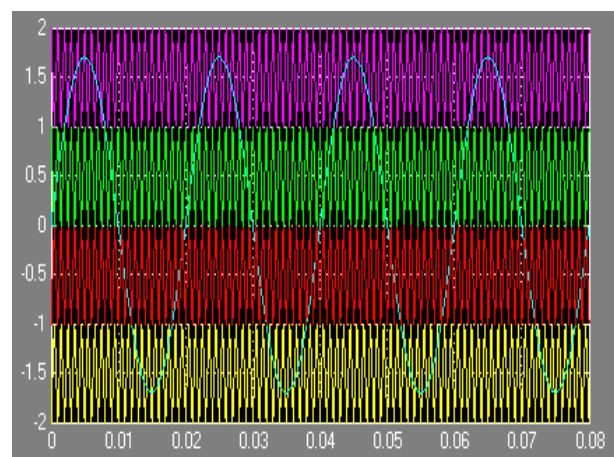


Fig.4 Multicarrier based PWM control scheme

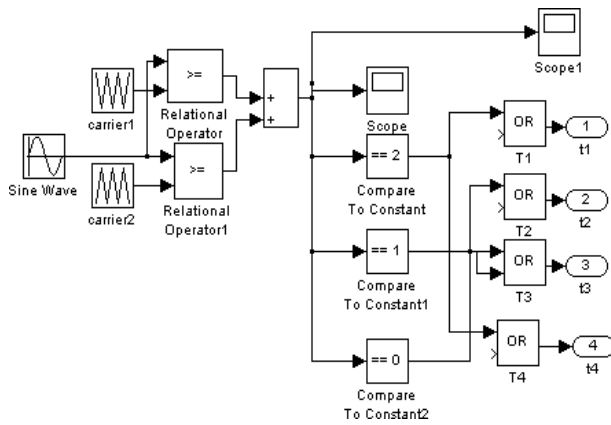


Fig.5 SPWM modulation scheme

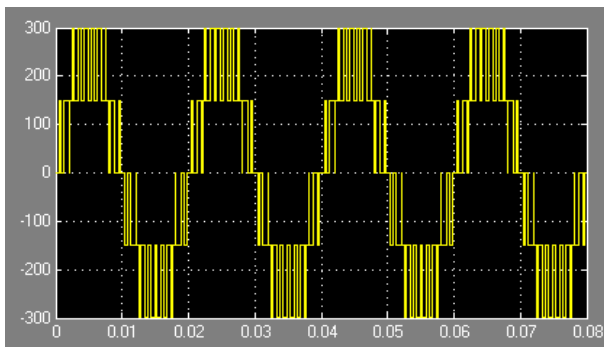


Fig.6 output voltage waveform of 5-level CHB based cascaded H-bridge inverter

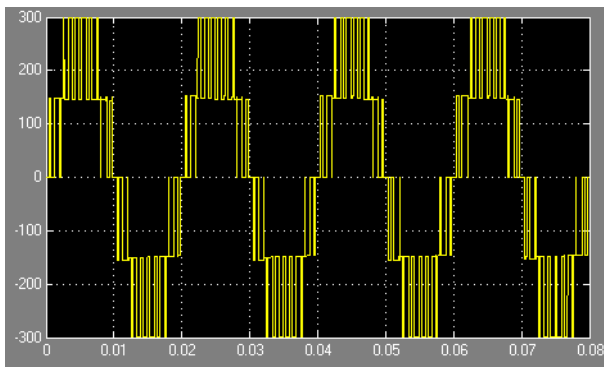


Fig.7 output voltage waveform of old TCHB 5-level inverter

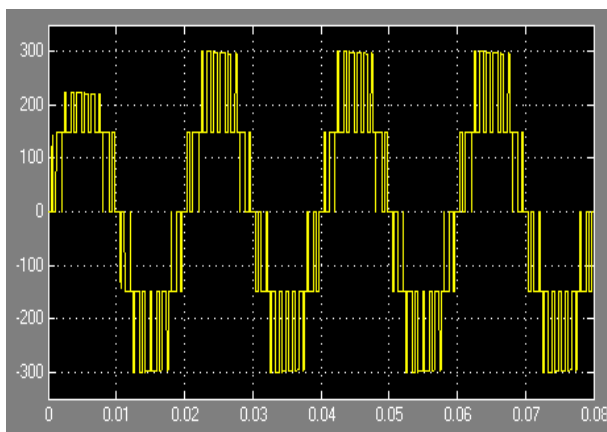


Fig.8 output voltage waveform of proposed TCHB 5-level inverter

VI. COMPARISON OF PROPOSED MULTILEVEL INVERTER WITH CASCADED H-BRIDGE TOPOLOGY

The purpose of research for the multilevel inverter includes to get a quality power output with the reduced number of switching devices, balancing of the capacitors, reduced number of clamping diodes in order to reduce the overall cost of the multilevel inverter. The two types of TCHB 5-level inverter are modelled for input DC voltage of 150V and their harmonic analysis is done on 5KHz. In the proposed TCHB 5-level multilevel inverter topology the number of switches are exactly similar to all other available topologies for 5-level except the inverter based on old TCHB only an extra bidirectional switch used. Also the input DC voltage source required is half of the voltage source rating required in the old TCHB inverter, conventional CHB and all other topologies for 5-level. To produce the same output voltage the CHB cascaded 5-level inverter requires two cells where as only one cell is required with the proposed TCHB topology. Fig.2 is showing the proposed single phase 5-level inverter which also represents a single power cell having input 150V DC voltage and the output ac voltage is 300V. The total harmonic distortion produced by the proposed new TCHB 5-level inverter is 35.39% only, Fig.11 shows the THD in % for single phase proposed TCHB 5-level multilevel inverter which is low as compared to old TCHB 5-level inverter by 3.27%. Fig.9 shows the THD in % for old TCHB 5-level multilevel inverter which is 38.66%. The CHB based 5-level single phase cascaded H-bridge inverter is having 37.63% THD which is 2.24% more than new TCHB 5-level inverter, Fig.9 shows the THD in % for single phase 5-level conventional H-bridge multilevel inverter. In order to produce the nine levels in the output voltage the cascaded H-bridge requires three cells where as the proposed topology requires only two cells

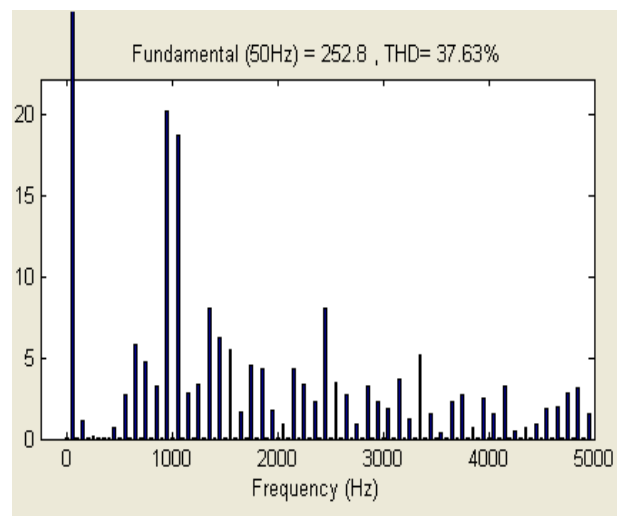


Fig.9 THD in % for single phase 5-level CHB based cascaded H-bridge multilevel inverter

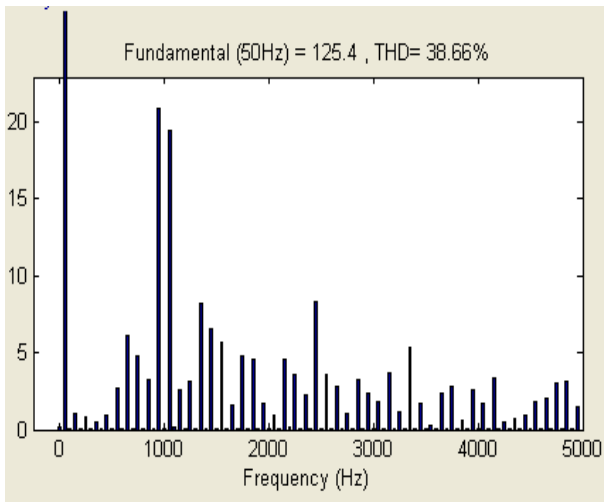


Fig.10 THD in % for single phase old TCHB based 5-level multilevel inverter

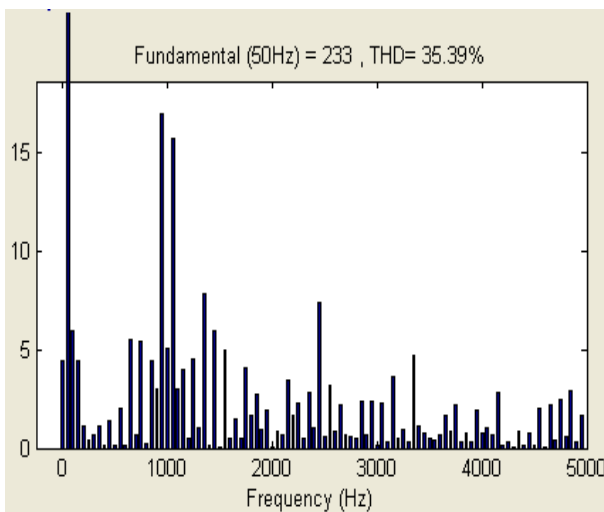


Fig.11 THD in % for single phase proposed TCHB based 5-level multilevel inverter

VII. CONCLUSION

The proposed TCHB 5-level multilevel inverter topology is much superior than both old TCHB 5-level inverter and conventional 5-level single phase cascaded H-bridge topology in terms of the total harmonic distortion and magnitude of the output voltage. The new TCHB 5-level inverter has less distortion of the output voltage compare to both the old TCHB and CHB cascaded 5-level inverter. In new TCHB more switching devices are used compare to old TCHB but their ratings are almost half for the same output voltage. For the same input voltage the output voltage of the new TCHB is more than old TCHB which is double of the input DC voltage. In comparison with diode clamped and the flying capacitor topologies for same number of level in output voltage waveform there is a great reduction in the diodes and the capacitors used.

REFERENCES

- [1] Y. S. Lai, F. S. Shy "New Topology For Hybrid Multilevel Inverter " Power Electronics. Machines and Drives, 16-18 April 2002, Conference Publication No. 487.0 IEE 2002.
- [2] Rashid, M.H, 2004. "Power Electronics: Circuits, devices and applications. Third Edition, Prentice Hall.
- [3] J. S. Lai, and F. 2. Peng, "Multilevel converters- A new breed of power converters". *IEEE Trans. On Ind. Appl.*, 32. 509-517; 1996
- [4] S.Mukherjee and G. Poddar, "A Series-Connected Three-Level Inverter Topology for Medium-Voltage Squirrel-Cage Motor Drive Applications," *IEEE Trans. Ind. Appl.*, vol. 46, pp. 179-186, 2010.
- [5] P. Lezana and G. Ortiz, "Extended Operation of Cascade Multicell Converters Under Fault Condition," *Industrial Electronics, IEEE Trans.Ind. Electron.*, vol. 56, pp. 2697-2703, 2009.
- [6] Ebrahim Babaei, 2008, "A Cascade Multilevel Converter Topology With Reduced Number of Switches" *IEEE Transactions on power electronics*, Vol. 23, No.6.
- [7] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Transactions on power electronics*, vol. 15, no. 4, July 2000, pp. 719-725
- [8] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive Control Algorithm Technique for Multilevel Asymmetric Cascaded H-Bridge Inverters," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 4354-4361, 2008.
- [9] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind.Electron.*, vol. 57, pp. 2553-2580, 2010.
- [10] J. Dixon and L. Moran, "High-level multistep inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron.*, vol. 21, pp. 330-337, 2006.
- [11] Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping Hew, "Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter with New Method of Capacitor Voltage Balancing" August 2, 2011; revised November 22, 2011 and February 27, 2012. Accepted for publication April 8, 2012.
- [12] Gupta, Krishna Kumar; Jain, Shailendra; , "A novel universal control scheme for multilevel inverters," *Power Electronics, Machines and Drives (PEMD 2012)*, 6th IET International Conference on , vol., no., pp.1-6, 27-29 March 2012
- [13] Gerardo Ceglia, Víctor Guzmán, Carlos Sánchez, Fernando Ibáñez, Julio Walter, and María I. Giménez "A New Simplified Multilevel Inverter Topology for DC-AC Conversion" *IEEE Transactions on Power Electronics*, Vol. 21, No. 5, September 2006.
- [14] Y. Zhang, J. He, S. K. Padmanaban, D. M. Ionel, "Transistor-Clamped Multilevel H-Bridge Inverter in Si and SiC Hybrid Configuration for High-Efficiency Photovoltaic Applications", *IEEE Energy Conversion*

Congress and Exposition, 2018, pp.2536-2542.

- [15] M Anzari, J Meenakshi, V T Sreedevi, "Simulation of a transistor clamped H-bridge multilevel inverter and its comparison with a conventional H-bridge multilevel inverter", International Conference on Circuits, Power and Computing Technologies, 2014, pp. 958-963.
- [16] N. B. Deshmukh, R. D. Thombare, M. M. Waware, D. S. More, "A novel family of three phase transistor clamped H-bridge multilevel inverter with improved energy efficiency", IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2016.
- [17] Eshet T. Wodajo, Malik Elbuluk, Seungdeog Choi, Haitham Abu Rub, "A ladder transistor-clamped multilevel inverter with high-voltage variation", IEEE Energy Conversion Congress and Exposition, 2017, pp. 5679-5684.
- [18] Nasrudin Abd. Rahim, Mohamad Fathi, Mohamad Elias, Wooi Ping Hew, Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter With New Method of Capacitor Voltage Balancing", IEEE Transactions on Industrial Electronics, Volume: 60, Issue: 8, 2013, pp. 2943-2956.
- [19] Subhashree Choudhury, Samikhya Nayak, Tara Prasanna Dash, P K Rout, "A comparative analysis of five level diode clamped and cascaded H-bridge multilevel inverter for harmonics reduction, Technologies for Smart-City Energy Security and Power, 2018.
- [20] Rahul Choudhary, Indrajit Sarkar, "Single phase five level Transistor Clamped inverter with multi-band hysteresis current control", IEEE International Conference on Power Systems, 2016. Indrajit Sarkar;B. G. Fernandes, "High resolution m-cell symmetric cascaded H-Bridge multilevel inverter with one transistor clamped H-Bridge per phase", IEEE Industrial Electronics Society, 2015, pp. 3399-3404.
- [21] M. F. M. Elias, N. A. Rahim, H. W. Ping, M. N. Uddin, "Asymmetrical transistor-clamped H-bridge cascaded multilevel inverter", IEEE Industry Applications Society Annual Meeting, 2012. Seok-Min Kim, Kyo-Beum Lee, "A Modified Third Harmonic Pulse-Width Modulation for Reduced Switching Loss in Cascaded H-Bridge Multilevel Inverters", IFAC Papers On Line vol. 52, no. 4, 2019, pp. 472-476
- [22] V. Kiranmayee, A. Sharath Kumar, "Performance Evaluation of Transistor Clamped H-Bridge (TCHB)-Based Five-Level Inverter. Innovations in Electrical and Electronics Engineering. Lecture Notes in Electrical Engineering, vol. 626., 2020, Springer, https://doi.org/10.1007/978-981-15-2256-7_16