Design of a Nine Stage Ring Oscillator Using PSO

Preeti Kumari[1], Madhuresh Suman[2]

[1]*Assistant Professor MIT Purnea,* [2]*Assistant Professor GEC Banka*

Abstract - Purpose of optimizing integrated circuits by hand becomes very thorny due to the complexity in the growth of Very Large-Scale Integrated (VLSI) circuits. Particle Swarm Optimization (PSO) is population-based meta-heuristic search algorithm. In this work, we have design a CMOS 9 stage Ring Oscillator (RO) consist of a series of nine CMOS inverter connected in a closed loop using three different sets of design parameter W_n , W_p and L for both NMOS & PMOS. On the basis of which phase noise, power and voltage waveform are obtained by using the technique CADENCE Virtuoso analog design environment.

Keywords - RO,PSO,FOM.

I. INTRODUCTION

Oscillating signals are seen in dissimilar types of electrical systems. An oscillating signal can be used as a clock signal in order to synchronize the operations of a digital electronic system. These signals can also be used in radio and communication systems.

Electronic oscillators are planned in order to create these signals. Phase Locked loops (PLLs) are normally used in almost every electronic system. CMOS Ring Oscillator (RO) is a necessary part of phase locked loops (PLL). The importance is quite intense these days, given the developments in the area of VLSI, ADCs, PLLs and VCOs have amazing usage of ring oscillators and ring oscillators are used in many applications such as integral frequency synthesis, clock and data recovery in communication systems and on chip clock distribution [1].

II. PARTICLE SWARM OPTIMIZATION (PSO)

Electrical oscillators are implemented within all types of electronic systems in the information, communication and sensor technology fields. PSO has roots in two main components methodologies. Perhaps more obvious are its ties to artificial life in general and to bird flocking, fish schooling and swarming theory in particular. PSO as developed by authors comprises a very simple concept and paradigms can be implemented in a few lines of computer code. It is demonstrated to execute well on genetic algorithm test functions [2]. The distinctions between the four main branches of evolutionary computation continue to blur [3]. Momentum factor restrict the particles inside the defined search space without checking the boundary at every iteration. The time varying acceleration coefficients reduce the cognitive component and increase social component [4].

III. NINE STAGE RING OSCILLATOR

A ring oscillator is realized by placing an odd number of open-loop inverting amplifiers in a feedback loop. The ring oscillator is the most widely manufactured integrated circuit of all. The ring oscillator is the most widely manufactured integrated circuit of all. Ring oscillators are being used by semiconductor foundries on every semiconductor wafer to observe the power dissipation, delay, jitter of fabricated CMOS inverters [5]. The Simplified structure of a ring oscillator is shown in Fig.1.

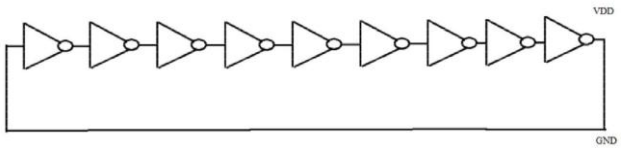

Fig.1 *Simplified structure of a ring oscillator*

IV. PHASE NOISE

Phase Noise is the noise increases at frequencies close to the oscillation frequency or its harmonics. The phase noise is generated by the thermal noise in ring oscillator. Phase noise is a continuous stochastic process representing random accelerations and decelerations in phase as an oscillator orbits at a nominally constant frequency in steady state [6].

V. FIGURE OF MERIT

The unit of FOM is dBc/Hz (*L* times a dimensionless factor). A smaller FOM corresponds to a better VCO [7]. A SR MPCG requires a reference clock with higher frequency, which can be realized in a power neutral way provided that the VCO core determines power consumption [8].

VI. SIMULATION RESULTS

Here complete simulation results are shown in this section. The CMOS 9 stage ring oscillators have been designed for three different sets of design parameter W_n , W_p and L for both NMOS & PMOS . On the basis of which phase noise, power and voltage waveform are obtained by using the technique CADENCE Virtuoso tool in 45nm CMOS technology. The schematic diagram of 9 stage ring oscillator is shown in Fig.2. The details results are tabulated in Table 1.

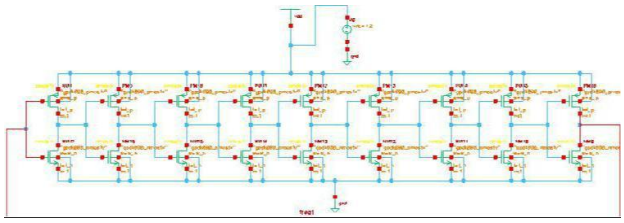

Fig.2 Schematic Diagram of 9 Stage Ring Oscillators

The simulated phase noise measurement, power measurement and waveform for design set-I of 9-stage RO is shown in Fig.3,4 and 5 respectively using CADENCE Virtuoso.

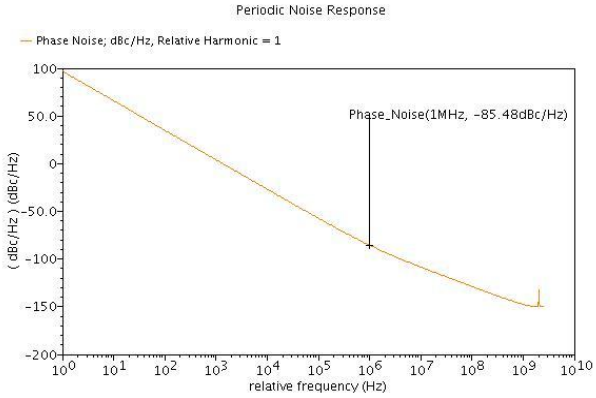

Fig.3 The Phase Noise measurement for set-I of 9-stage RO

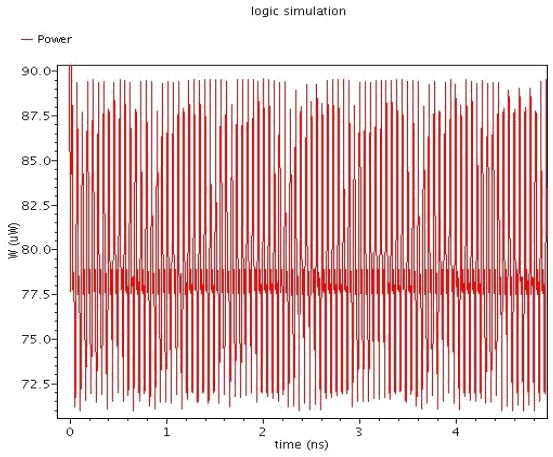

Fig.4 The *Power measurement* for set-I of 9-stage RO

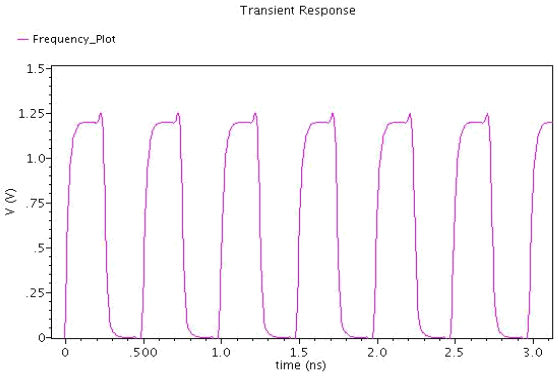

Fig.5 The output waveform for set-I of 9-stage RO

The simulated phase noise measurement, power measurement and waveform for design set-II of 9-stage RO is shown in Fig.6,7 and 8 respectively using CADENCE Virtuoso.

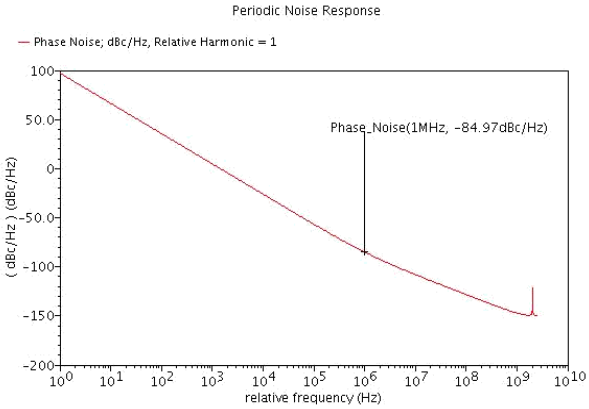

Fig.6 The Phase Noise measurement for set-II of 9-stage RO

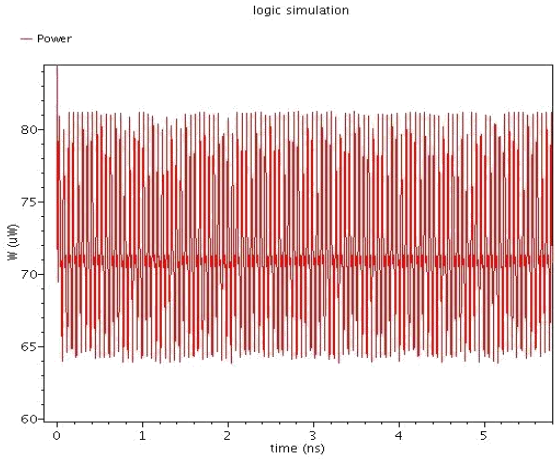

Fig.7 The *Power measurement* for set-II of 9-stage RO

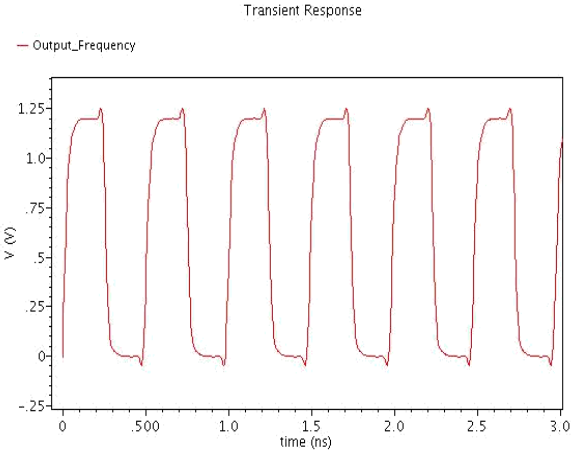

Fig.8 The output waveform for set-II of 9-stage RO

The simulated phase noise measurement, power measurement and waveform for design set-III of 9-stage RO is shown in Fig.9,10 and 11 respectively using CADENCE Virtuoso.

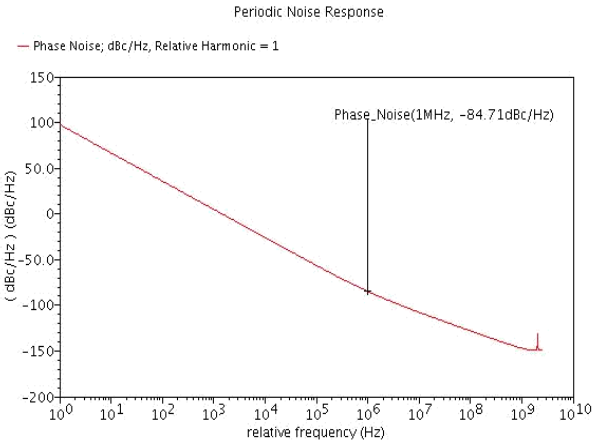

Fig.9 The Phase Noise measurement for set-III of 9-stage RO

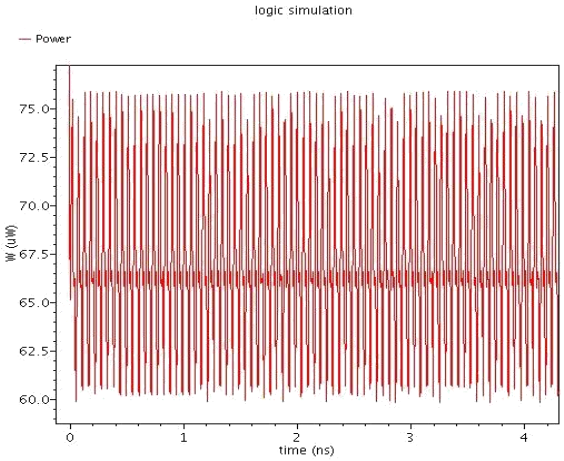

Fig.10 The *Power measurement* for set-III of 9-stage RO

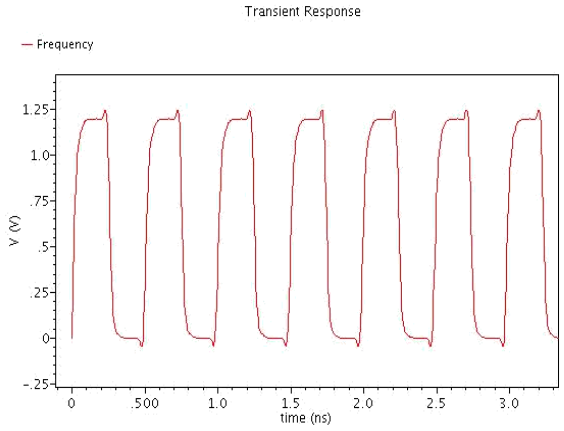

Fig.11 The output waveform for set-II of 9-stage RO

VII. CONCLUSION

We design a nine stage CMOS ring oscillator circuit consist of a series of nine CMOS inverter connected in a closed loop. The value of design parameter W_n , W_p and L for both NMOS & PMOS transistors obtained from PSO. On basis of which phase noise, power and voltage waveform are obtained by using the technique CADENCE Virtuoso analog design environment and the observed frequency of oscillation are of value 2.02GHz, 2.027GHz and 2.02227GHz respectively, having a nominal deviation from the desired frequency of 2 GHz. We also calculate the value of figure of merit (FOM) for the three sets of design parameters which are - 162.5561, -162.5337 and -162.5660 respectively.

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AUTHOR'S PROFILE

Preeti Kumari has received her B.Tech in Electronics & Communication Engineering from Millia Institute of Technology, Purnea in the year 2010 and M.Tech in Microelectronics and VLSI Design from Haldia Institute of Technology, Haldia affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT) Kolkata in the year 2015. At present she is working as an Assistant professor at Millia Institute of Technology, Purnea (BIHAR). Her areas of interests are VLSI Design, Communication and Antenna.

Madhuresh Suman has received his B.Tech in Electronics & Communication Engineering from Haldia Institute of Technology, Haldia affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT) Kolkata in the year 2013 and M.Tech in Microelectronics

and VLSI Design from Haldia Institute of Technology, Haldia affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT) Kolkata in the year 2015. At present he is working as Assistant professor at Government engineering College, Banka(BIHAR). His areas of interests are VLSI Design, Communication and Antenna.

Table-1: Design Parameter and performance of nine stage ring oscillator

Design Set	Predicted by PSO			Measured using CADENCE Virtuso ADE			
	W_n(nm)	W_p(nm)	L(nm)	Power (µwatt)	Phase Noise (dB/Hz)	Frequency (GHz)	Figure of Merit
I	220.554	370.556	172.518	80.00	-85.48	2.0200	-162.5561
II	202.220	330.750	172.407	72.00	-84.97	2.0270	-162.5337
III	188.654	310.824	172.609	67.00	-84.71	2.0227	-162.5660