Designing of SRAM Cell Organization To Reduce Leakage Current

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Abstract- Today's battery mobile applications demand for devices with low power, high dense and high performance. The VLSI industry is continuously following a down path for CMOS devices technology and as the technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased as a result of shrinkage in transistor size. Increase in number of transistor on chip increase the heating effect in the chip. To minimize this heating effect, the supply voltage, being one of the critical parameters, has also been reduced. Therefore, in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. However, aggressive scaling has resulted in devices with very low threshold voltage and very thin oxide layer.

I. INTRODUCTION

To satisfy the low power dissipation criteria the supply voltage, being one of the critical parameters, has also been reduced. Therefore in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. However aggressive scaling has resulted in devices with very low threshold voltage and very thin oxide layer [3]. These devices with very low threshold voltage and very thin oxide layer presented the one of the biggest challenges of VLSI industry – power integrity closure. Increase in power dissipation as shown in Figure 1.3 give rise to this challenge [4].

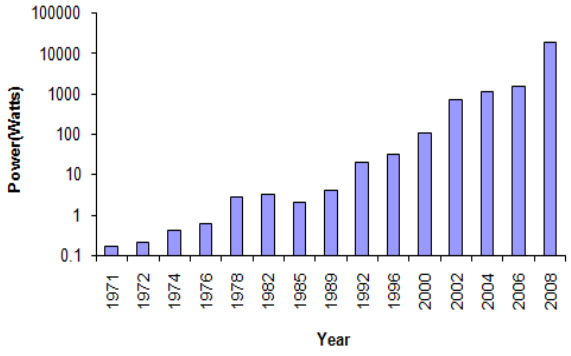


Figure 1 Power Dissipation in VLSI Circuits

Classification of Power Dissipation

Power dissipation in CMOS devices can be boardly classified in two catogries – active power and standby power as illustrated in Figure 1.4. Power dissipated during active state of devices is kwown as active power and power dissipated during idle state of devices is known as standby power. Active power can be further classified as – static power and dyanmic power.

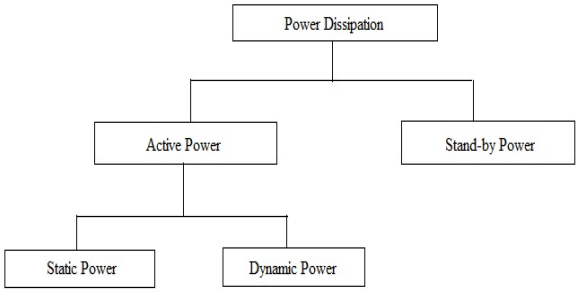


Figure 2 Classification of Power Dissipation

1.2.1 Static Power

It is also known as cell internal power. Cell internal power is power dissipated by the momentry short circuit between the power source and ground when a circuit switches [5].Short circuit current Isc is the source of internal power.Cell internal power is below 10-15% of total power dissipation and it can be formulated as-

$$P_{internal} = I_{sc}.V_{DD}$$

1.2.2 Dynamic Power

Dynamic power is consumed as capacitances, wires, etc. are charged and discharged, or in other words, as design signals transition. It is also known as switching power. This is the dominant component of active power. Traditionally dynamic power is the main source of the power dissipation in the circuits [6]. For any given signal within a design, the average amount of dynamic power consumed can be formulated as:

$$\boldsymbol{P_{leakage} = I_{lk}.V_{DD}}$$

1.2.3 Standby Power

Standby power is the power dissipated all the time, even when a circuit is held in steady state.Because the MOSFET is not a ideal switch, so leakage current Ilk exist [7]. Leakage power can be formulated as:

1.3 Leakage Current Components

Leakage current is mainly contributed by various leakage mechanisms such as reverse bias PN junction leakage, sub-threshold leakage, gate oxide tunneling current, gate

current due to hot carrier injection, channel punch through current, gate induced drain leakage [8]. However due to aggressive scaling three main components which dominant the others are shown in Figure 1.6.

- Sub threshold leakage current
- Junction leakage current
- Gate leakage current

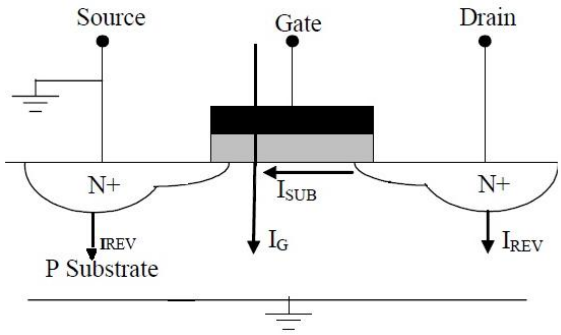


Figure 3 Major leakage current components

II. LITERATURE REVIEW

There are various leakage current reduction techniques for SRAM cell at either circuit level or architecture level which are based on the techniques such as multi threshold voltage, dynamic threshold, voltage scaling, and transistor stacking effect in CMOS circuits. These techniques reduce either active (dynamic and static) or standby power dissipation in SRAM cell [11].

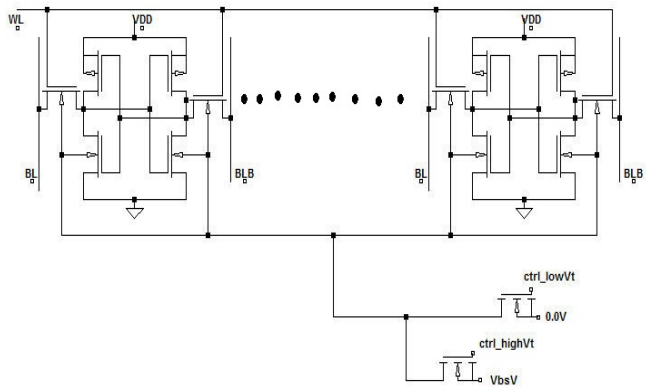


Figure 4 Dynamic Vth SRAM

III. SIMULATION SETUP

We used integrated circuit front to back full design (icfb) cadence tool for our design. Technology file and various tools of it used for simulation and layout are given in the below table.

Classification	Tool	Version
Technology File	UMC	90nm
Schematic Entry	Cadence Composer	5.1.41_ISR
Simulation Interface	Cadence Analog Design Environment	5.1.41_ISR
Simulation Tool	Cadence Spectre	5.1.41_ISR
Layout Editor	Cadence Virtuoso	5.1.41_ISR
DRC Tool	Cadence Assura	3.1.7
LVS Tool	Cadence Assura	3.1.7
Parasitic RC Extractor	Cadence Assura	3.1.7

3.1 Technology File :- We used UMC 90nm technology file along with analogLib and basic libraries of the Cadence tool for our design. This technology file includes list of components, DRC rule check file, LVS rule check file, LPE rule check file and layer mapping table. We used N_10_SP and P_10_SP models for NMOS and PMOS respectively.

3.2 Cadence Schematic Composer A schematic design is a graphical representation of a logic circuit design. Pins, wires and instances are used to complete the schematic. Cadence virtuoso schematic editor provides numerous capabilities to facilitate fast and easy design entry, including design assistants that speed common tasks. Well-defined component libraries allow faster design at both the gate and transistor levels. Sophisticated wire routing capabilities further assist in connecting devices. For larger and more complex designs, Virtuoso schematic editor not only supports multi-sheet designs but also provides the ability to design hierarchically, with no limit on the number of levels used. The Hierarchy Editor makes hierarchical designs easy to traverse, and automatically ensures all connections are maintained accurately throughout the design [19].

3.3 Cadence Analog Design Environment Cadence virtuoso analog design environment is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to center designs better for yield improvement and advanced matching and sensitivity analyses. By supporting extensive exploration of multiple designs against their objective specifications, Virtuoso analog design environment sets the standard in fast and accurate design verification [19].

3.4 Cadence Spectre Simulator Spectre is an advanced circuit simulator that simulates analog and digital circuits at the differential equation level. The basic capabilities of the Spectre circuit simulator are similar in function and application to SPICE, but the Spectre circuit simulator is not descended from SPICE. The Spectre and SPICE simulators use the same basic algorithms—such as implicit integration methods, Newton- Raphson, and direct matrix solution—but every algorithm is newly implemented. Spectre algorithms result in an improved simulator that is

faster, more accurate, more reliable, and more flexible than previous SPICE-like simulators.

3.5 Cadence Virtuoso Layout Editor We used cadence design framework II (DFII) workbench for layout. Virtuoso Layout XL accelerates custom layout with a comprehensive set of user-configurable, easy-to-use pure polygon layout features within a fully hierarchical environment. Virtuoso Layout XL is driven by a connectivity source from Virtuoso Schematic Editor or a netlist such as CDL or SPICE. A layout vs. schematic (LVS)-correct layout can then be created, ensuring correct-by construction layout, higher productivity, and shorter verification time. Virtuoso Layout XL automates tedious design tasks such as device generation, placement, and routing. We can cross probe schematics and layout to highlight instances and devices, as well as quickly identify unconnected nets.

4.1 SRAM Cell Organization :- Traditional SRAM is formed by group of six transistors along with a number of other peripheral devices such as row decoder, column decoder, sense amplifier, and write circuitry etc. [20] as shown in Figure 4.1.

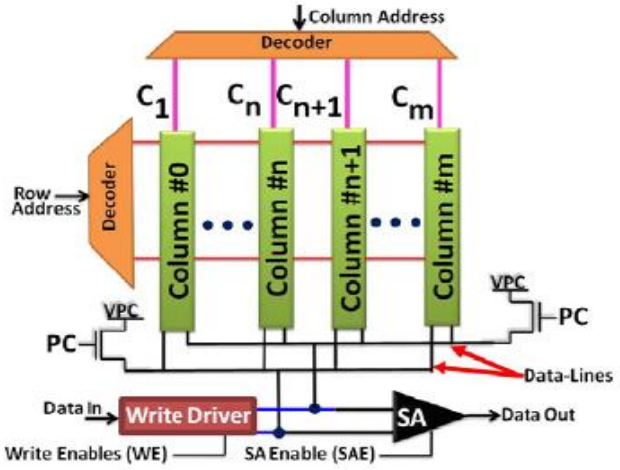


Figure 4.1 SRAM organization

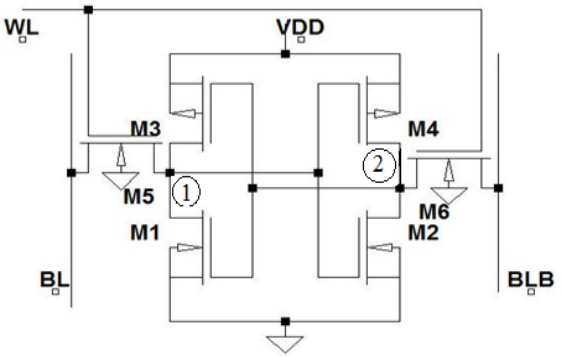


Figure 4.2 6T CMOS SRAM Cell

4.2 6T CMOS SRAM Cell A low power SRAM cell may be designed simply by using cross coupled inverters. The stand-by power consumption of the memory cell will be limited to relatively small leakage currents of both CMOS inverters. The only drawback of using the cross coupled inverters, is slightly larger area than that of the other alternatives (resistive load, depletion-load NMOS SRAM Cell). The circuit structure of full CMOS static RAM is shown in Figure 4.2.

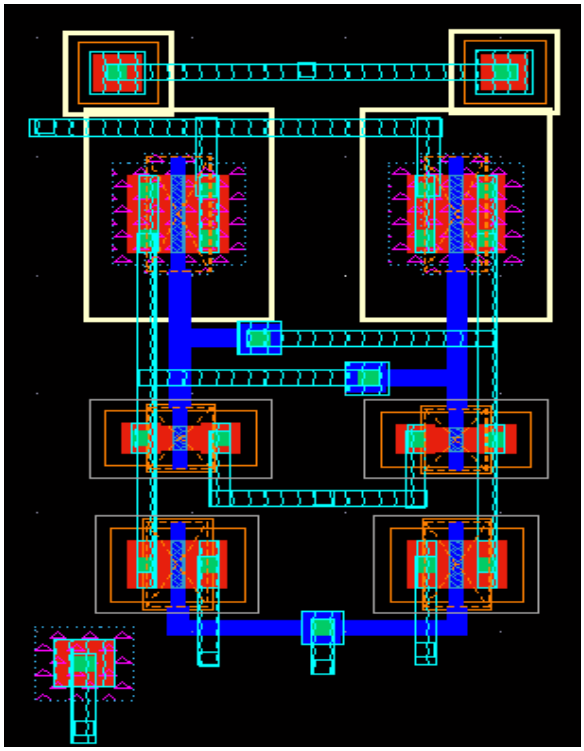


Figure 4.3 Layout of full CMOS SRAM Cell

Write Margin of CMOS SRAM Cell :- Write margin quantifies the stability of RAM cell during the write operation. Smaller the value of write margin, harder it is to write the cell. Therefore, along with higher SNM and read margin SRAM cell should have higher write margin. There are various ways to calculate the write margin of the SRAM cell such as “butterfly” curve approach, bit line sweeping, Word-line sweeping and use of the N-curve approach [25]. We calculated the write margin of the SRAM cell using the bit-line sweeping method. The 6T SRAM cell is configured as shown in the Figure 4.13 for a write ‘1’ case.

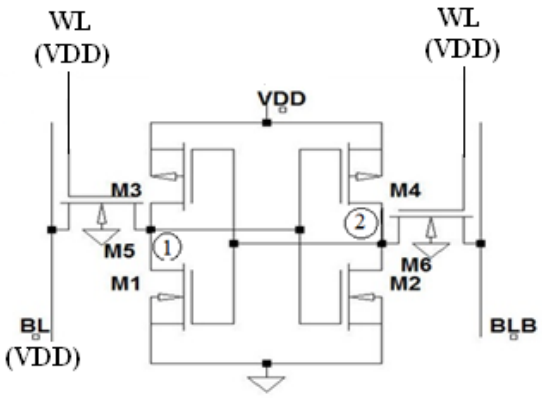


Figure 4.13 Circuit for sweeping BL to get write margin

4.3 Row Decoder A 1-out of -2M decoder is nothing less than a collection of 2M complex, M input, logic gates. Each of the outputs WL is a logic function of the M input address signals. For example if 8 input address (A0 to A7) is used then WL0 and WL127 can be enabled by the following

following

$$WL_0 = \overline{A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7}$$

$$WL_{127} = \overline{A_0} A_1 A_2 A_3 A_4 A_5 A_6 A_7$$

Decoder can be broadly classified in two categories – static decoder and dynamic decoder [20].

4.3.1 Static Decoder In this type of decoder a complex gate is splited into two or more logic layers to produce both faster and a cheaper implementation. This decomposition concept makes it possible to build fast and area efficient decoder. The first segment is known as pre-decoder and the second one produces the final word-line signals [20]. For example an 8 input NAND decoder can be regrouped in following way:

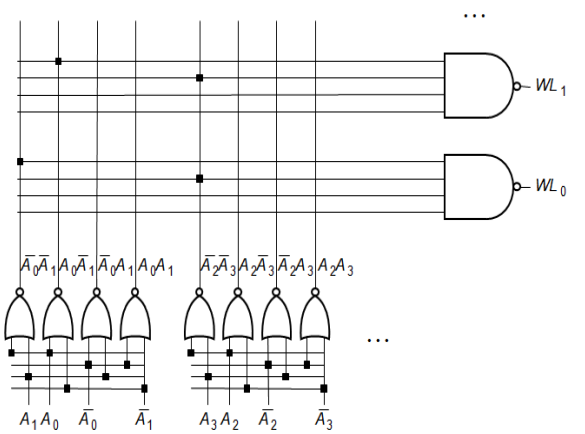


Figure 4.19 Hierarchical row decoder

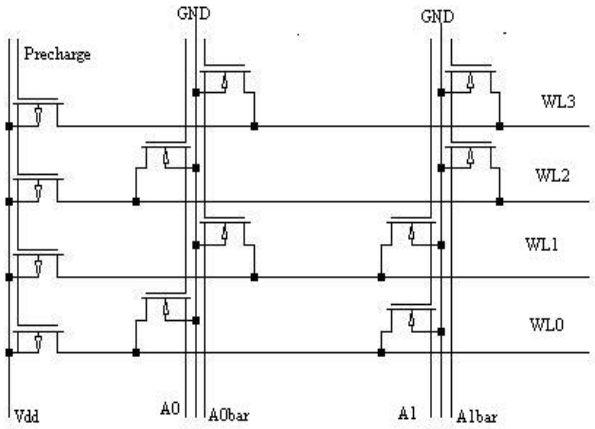


Figure4.20 2-to-4 NOR Decoder

4.3.2 Dynamic Decoder Since only one transistor determines the decoder speed, it is interesting to evaluate other circuit implementations. Dynamic logic offers a better alternative. The decoder can be either implemented as NOR array or NAND array. NOR array will consumes more area as compares to NAND array, but it will be faster [20].

4.3.3 Column Decoder Column decoder used should match the bit line pitch of the memory array. The functionality of a column and block decoder is similar to a 2K-input multiplexer, where K stands for the size of the address word. The column decoder can either be separated or shared between the read and write operation. During the read operation, they have to provide the discharge path from the pre-charged bit line to the sense amplifier. When performing a write operation to a memory array, they have to be able to drive the bit line low to write a '0' in the memory cell [20]. One configuration which utilizes only NMOS is shown in Figure 4.22.

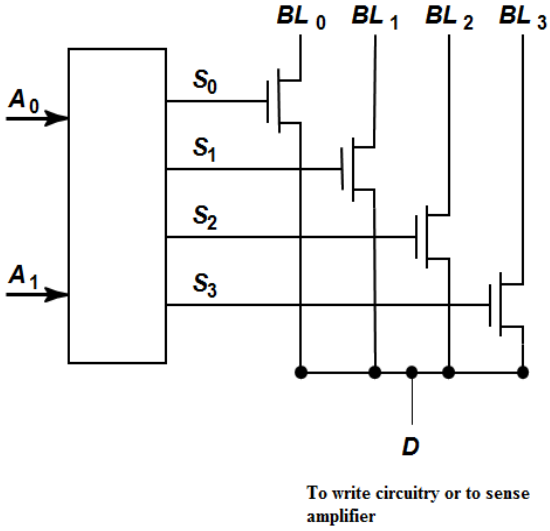


Figure 4.22 Column decoder

4.3.4 Address Transition DetectionAddress transition detection block is used to generate the clock pulse for the SRAM. The block diagram of the ATD (address transition detection) is shown in the Figure 4.23. Whenever there is change in the address signal, the ATD block generates the clock pulse.

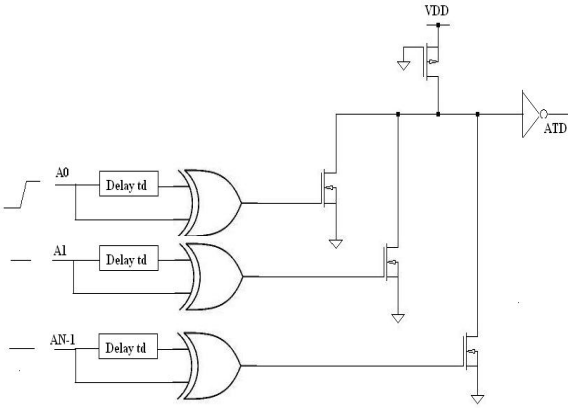


Figure 4.23 Address transition detection block

4.1 Proposed Work :- Our proposed work includes the benefits of both Drowsy scheme and Dynamic Vthcontrol scheme. A SRAM cell which is not accessed for a certain time period will be assigned high Vth and reduced stand-by voltage, and SRAM cell which is in frequent use will be assigned low Vth and normal VDD. Figure 5.1 shows the schematic and waveforms of a time based scheme, used to do this job.

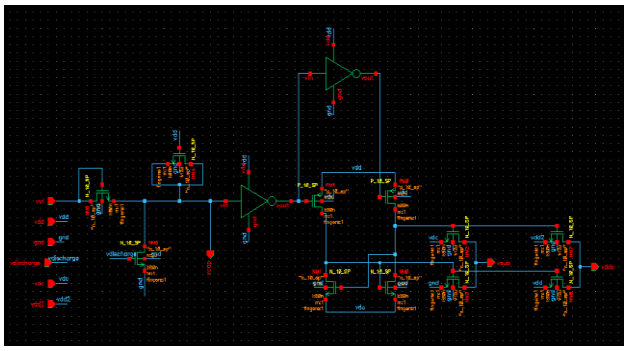


Figure 5.1 (a) Schematic diagram of proposed technique

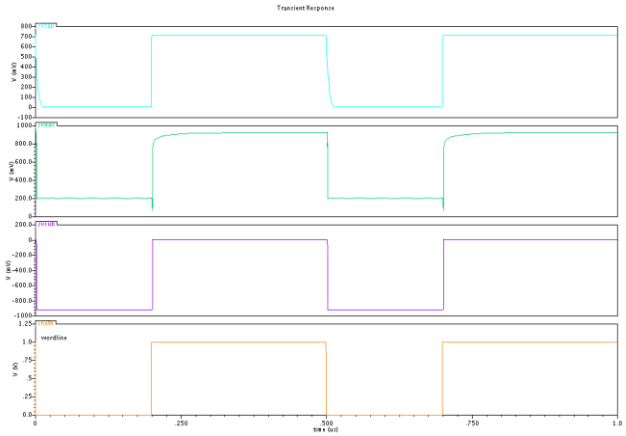


Figure 5.1 (b) WL, Vcap, Vsub and Vddc voltage waveforms for the control circuit

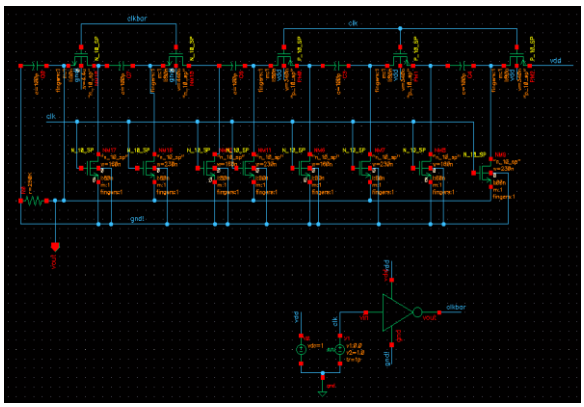


Figure 5.3 (a) Schematic of five stage switch capacitor DC to DC converter

In stand-by mode SRAM cell just acts like a flip flop and used only to preserve the data stored. So we can reduce the power supply to data retention voltage (DRV) to minimize the power dissipation. However in an actual implementation, reducing VDD al the way to DRV is not really a good option, as other mechanism such as noise on power supply voltage may disrupt the state of memory cell. To offset these effects, an appropriate noise margin has to be provided. We provide a guard band of 135mv above DRV (=65mV) and used five stage switch capacitor converter [14] to convert VDD of 1V to 200mV. Figure 5.3 shows the schematic of switch capacitor converter and its output.

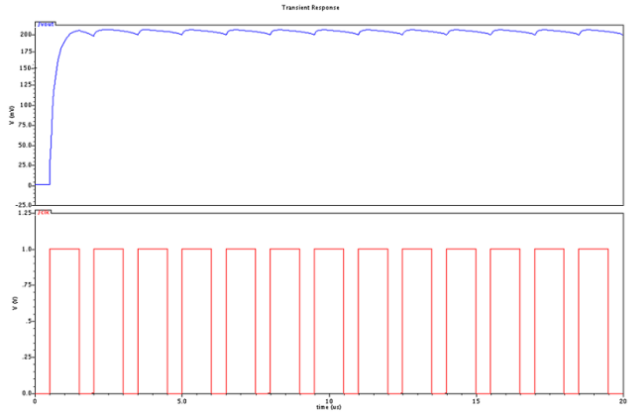


Figure 5.3 (b) output of five stage switch capacitor DC to DC converter

IV. SIMULATION & RESULTS

Figure 6.1 shows the simulation results for write '0', read '0' and write '1' and read '1' operations, when no technique is being applied.

Case	Average Power(W)	Delay (ps)	
		Read	Write
'0' case	4.19e-08	942.935	27.2
'1' case	1.23e-06	820.007	34.6

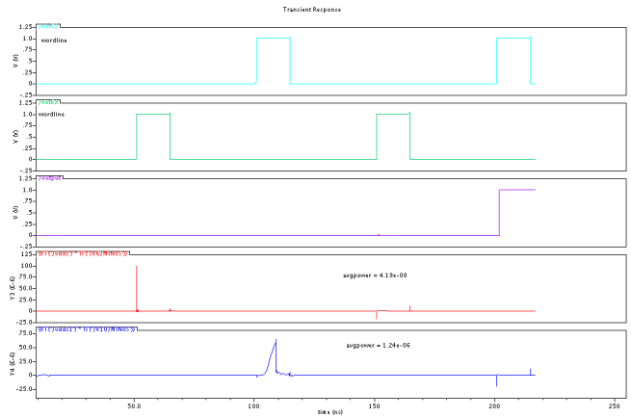


Figure 6.1 Simulation Result for conventional 6TSRAM cell

Data Retention Gated Ground Scheme

Table shows the results for 6T conventional SRAM cell with DRG technique applied to it and Figure 6.2 shows the graphical representation of simulation result for it.

Case	Average Power(W)	Delay (ps)	
		Read	Write
'0' case	3.61e-08	952.766	30.181
'1' case	6.85e-07	822.672	36.211

Table 6.2 Simulation Result for Conventional SRAM Cell with DRG Technique applied

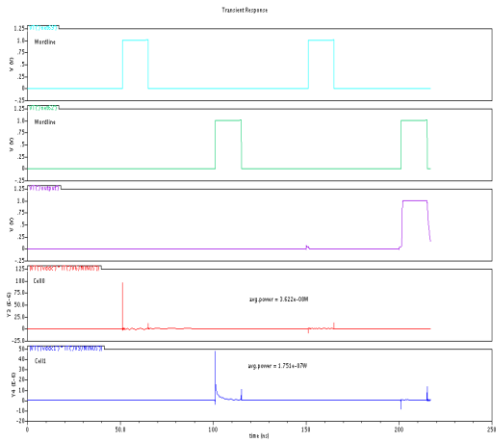
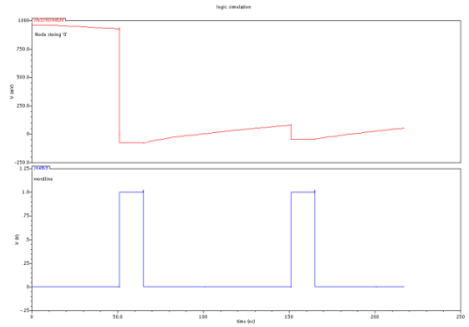
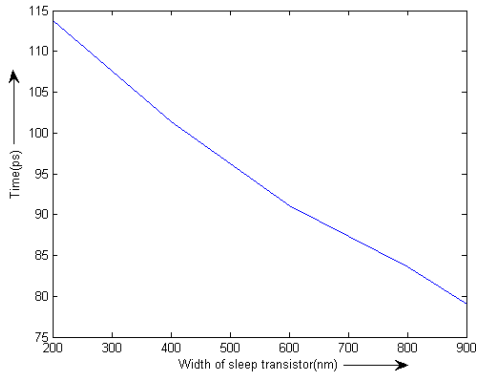


Figure 6.2 Simulation Result for Conventional SRAM Cell with DRG Technique applied

It is found that voltage level at node storing "0" gets strapped to a small positive voltagewhen the word line was low and restored back to zero when word line is enabled as shown in Figure6.3 (a) level of this strap voltage vary with the size of sleep transistor as shown in Figure 6.3 (b).



(a)



(b)

Figure 6.3 (a) Strap voltage of node storing '0' (b) Strap voltage level Vs sizing of sleep transistor

Sizing of the gated ground transistor also affect the amount of average dissipated power and delay of the memory cell. Figure 6.4 (a) and (b) respectively show the variation of average dissipated power and delay of memory cell (read '0') for different sizing of sleep transistor.

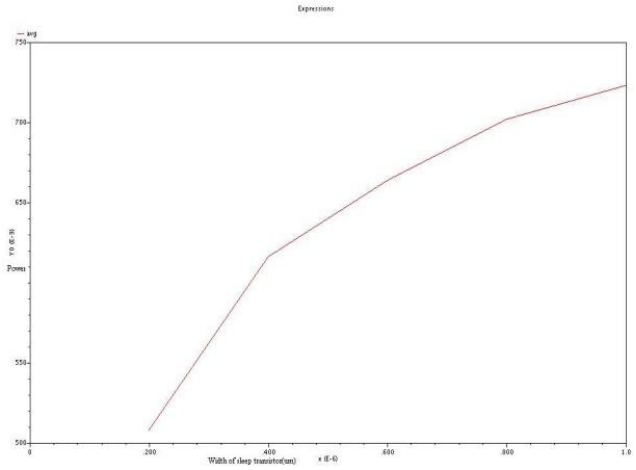


Figure 6.4 (a) Average power dissipated Vs sizing of sleep transistor

It is found that average power dissipation increased with reducing the size of the sleep transistor however delay of the memory cell decreased. So, there is trade of between saving of average power dissipation and delay of memory cell for a given sizing of sleep transistor and we have to properly size the sleep transistor depending upon the optimization parameter.

Conclusion :- Power waveforms show that there is consumption of power when there is no initialization of SRAM cell. The read, write and data retention are happening correctly for all the techniques applied to SRAM cell. Table 7.1 compares all the techniques for average power dissipation and delay of SRAM cell.

Technique	Average power dissipation(W)		Delay(ps)	
	'0' Case	'1' Case	Read '0'	Write '0'
Simple 6T SRAM	4.19e-08	1.23e-06	942.935	27.2
DRG Scheme	3.61e-08	6.85e-07	952.766	30.181
Asymmetric SRAM	3.19e-08	4.565e-07	967.49	31.357
Dynamic Vth SRAM	4.07e-08	1.08e-06	943.125	28.057
Drowsy Scheme	3.45e-08	2.13e-07	3680.73	197.321
Proposed technique	2.38e-08	6.87e-08	4625.89	376.452

After multiple iteration it is found that DRG technique significantly reduce the leakage current but voltage level at node storing "0" get strapped to small positive value and a small noise can destroy our data stored. It also found that by varying the sizing of gated ground transistor the data retention capability of SRAM cell varies along with the variation in leakage power saving. However DRG with clamp diode beside the significant reduction in leakage current also improves the noise immunity of SRAM cell. Leakage power saving and small magnitude of strap voltage depend on the threshold voltage of the MOSFET used for diode. By making the SRAM cell asymmetric we were able to reduce the average power dissipation with little increase in delay. Performance of SRAM cell is not affected by using the dynamic Vth control scheme since most of the access will be on low Vth SRAM. Leakage energy is saved for the SRAM cells which are in idle mode.

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