

# A Novel Delay & Quantum Cost Efficient Reversible RAM - A Review

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**Abstract-** *There exists a growing body of explorations about Computer Aided Design of reversible and quantum circuits. Most of these explorations are related to designing and optimizing circuits in binary quantum computing. Quantum circuits and computers, the recently invented breakthrough technology that is praised as a leading future technology by top specialists. The ability to trap ions in three dimensional space has contributed to many advances in atomic physics, laser cooling, and atomic clocks, as well as applications such as mass spectrometers. Quantum technology is inherently reversible and is one of the most promising technologies for future computing systems. In addition to reversibility, it has powerful properties such as quantum superposition, quantum parallelism and quantum entanglement that allow for solving problems much more efficiently than in classical computing. There was a growing interest in the quantum and particle Physics research communities in the realizations and applications of d-level quantum systems (a different name used by them for multiple-valued quantum logic circuits). Some results from classical ternary logic and reversible ternary logic can be adapted. On the other hand, new important properties can be analyzed.*

**Keywords –** *Quantum computing, Reversible logic, Reversible D-FF; Reversible Decoder; RRRAM.*

## I. INTRODUCTION

Since ancient times, humanity has been seeking tools to help us perform tasks which involve calculations. Such are computing the area of a land, computing the stresses on rods in bridges, or finding the shortest route from one place to another. A common feature of all these tasks is their structure:

*Input – – – → Computation – – – → Output*

The computation part of the process is inevitably performed by a dynamical physical system, evolving in time. In this sense, the question of what can be computed is intermingled with the physical question of which systems can be physically realized. If one wants to perform a certain computation task, one should seek the appropriate physical system, such that the evolution in time of the system corresponds to the desired computation process. If such a system is initialized according to the input, its final state will correspond to the desired output.

Resilient quantum computation is more complicated than simply protecting quantum information which is sent

through a noisy quantum channel. Naturally, to protect the information we would compute on encoded states. There are two problems with noisy computation on encoded states. The first is that the error correction is done with faulty gates, which cause errors themselves. We should be careful that the error correction does not cause more harm than it helps. The second problem is that when computing on encoded states, qubits interact with each other through the gates, and these way errors can propagate through the gates, from one qubit to another. The error can spread in this way to the entire set of qubits very quickly.

The applications of Grover's algorithm to solve various NP-hard problems changes by designing new oracles for them, so the question is how to design these oracles at all, and more importantly how to design them efficiently. The permutative circuits that are not oracles have the same number of inputs and outputs, and the inputs are not necessarily repeated on outputs, as it is required in oracles. They are useful to build parts of oracles. For instance the spectral transforms, arithmetic blocks, image processing blocks, calculations of cost functions, "counting number of ones in input vector" and many other similar tasks (that are normally built into the data path of a standard or signal processing computer) all belong to this group. We also deal with fast quantum transforms, another important class of algorithms by itself, used for instance in the famous Shor's algorithm or in those quantum computers for vision which use the Fast Quantum Fourier Transform. Thus the research covers design of two kinds of blocks so far used in quantum computing: binary and multiple-valued.

A variety of combinatorial problems and will become a basis of future intelligent robotic and media systems. To aid in inventing these future algorithms a new multi-valued quantum logic system is invented and investigated in this research. I introduce Galois Field and Controlled Gate quantum logics. These new logic algebras should be of interest to the quantum logic synthesis community because of their analogies and extensions to the classical Reed-Muller Logic and classical reversible logic of Feynman, Toffoli and Fredkin [Feynman82, Fredkin82, Toffoli90, Feynman96], and hence their properties of high testability. Biamonte and Perkowski extended the classical Reed-Muller logic algorithm based synthesis method of Reddy to quantum circuits, using an equivalent of Positive

Polarity Reed-Muller logic. Sarabi and Perkowski [Perkowski92a, Perkowski95], Sasao, Bhattacharya and others generalized the results of Reddy and Pradhan to more complex circuit structures than Positive Polarity Reed-Muller forms. In this research I will show how Kronecker Decision Diagrams and Lattices, Fixed Polarity Reed-Muller forms (FPRM), Generalized Reed-Muller forms (GRM), and Exclusive-Or- Sum-of-Products (ESOP) binary circuits can be generalized to multiple-valued quantum circuits. I will discuss classes of MV expansions, canonical forms, trees and diagrams as well as corresponding flattened expressions and circuits in their quantum realizations.

Design implementation of multiple-valued quantum circuits with quantum arrays using multiple-valued Muthukrishnan-Stroud gates [Muthukrishnan00] in Ion Trap and similar technologies recently became practically possible. Moreover, based on generalizations of binary circuits to multiple-valued circuit families shown in the literature. However, the algorithmic complexity of synthesizing large circuits of this type exceeds by far the complexity of designing classical circuits. Efficient heuristic methods of synthesizing them are therefore necessary.

Reversible circuits have been studied extensively to find an alternative solution to classical design. Some unique properties of reversible logic are identified to facilitate the synthesis and testing of circuits and above all their applications in different arena of computation. The quantum realizations of reversible gates are exercised to relate reversible logic to quantum circuits. In this chapter, we will present the basic definition and properties of reversible function, gate design and circuit construction followed by the cost parameters of reversible circuits.

It is sometimes more convenient to use another universal model, which is polynomially equivalent to Turing machines, called the Boolean circuit model. We will use the quantum analog of this model throughout this research. A Boolean circuit is a directed acyclic graph, with nodes which are associated with Boolean functions. These nodes are sometimes called logical gates. A node with  $n$  input wires and  $m$  output wires is associated with a function  $f : \{0,1\}^n \rightarrow \{0,1\}^m$ . Here is a simple example:

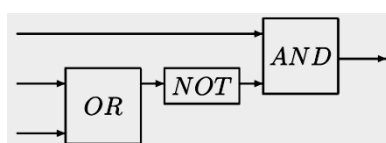


Figure1.1 An example of Boolean circuit function.

Given some string of bits as input, the wires carry the values of the bits, until a node is reached. The node

computes a logical function of the bits (this function can be NOT, OR, AND, etc.) The output wires of the node carry the output bits to the next node, until the computation ends at the output wires.

## II. SYSTEM MODEL

### A. Reversible function

A  $n \times n$  reversible circuit realizes an  $n$ -input/ $n$ -output function where each input vector maps bijectively to a unique output vector. The reversible circuits allow no fan-out and no feedback path. The cascading preserving these two rules can build any reversible circuit from reversible gates.

Table 1 Truth – Table of a full adder (adding insufficient) garbage.

$C_{in}$	A	B	carry	sum	g
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	-
1	0	1	1	0	1
1	1	0	1	0	-
1	1	1	1	1	1

Irreversible functions differ from their reversible counterpart in two aspects. First, the number of inputs and outputs are generally not equal, and secondly the input and output mapping is not unique, i.e., the same output pattern can occur for different input combinations. Therefore, some processing is required to transform an irreversible function into a reversible one. A simple addition of extra variables as outputs to match the number of inputs is generally not sufficient, as this process does not guarantee reversibility. Additionally, we need to confirm unique output pattern. For example, consider the truth table of a full adder. The adder has three inputs and two outputs: sum and carry. Even if we add one output to make input-output number the same, then the specification does not become reversible as output patterns 01 and 10 repeat. Hence, we need to add more outputs to make the circuit reversible. for example in table 1 truth table for a full adder .

Thus reversible synthesis from irreversible specification aims to embed an arbitrary irreversible function of  $I$  inputs

and O outputs (generally  $I \wedge O$ ) into a reversible circuit, constructed solely from reversible gates. The added A inputs are referred as ancilla bits and the extra G outputs are garbage bits. The lower bound on the number of extraneous bits G is based on the number of repetitions M of identical output combinations. The minimal number of added garbage bits,  $G = \lceil \log_2 M \rceil$ . Then, the number of ancilla bits A is such that  $I + A = O + G$ . For example, in Table 2

Observe in the irreversible specification of adder circuits ( $I = 3$  and  $O = 2$ ), the maximum number of output patterns (01 or 10) repeated is 3. So, we need to add extra bits at output,  $G = 2$  (garbage) The ancilla bits can be set to constant 0 or 1 by the designer. Garbage outputs can have any value following the reversible constraint, i.e. no output pattern is repeated in the specification.

Table 2 Reversible embedding of full adder.

$a_1$	$C_{in}$	A	B	carry	sum	$g_1$	$g_2$
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	1	0	0	0
0	1	0	0	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	1	1	0

### B. Reversible gates

Given a reversible specification, there exists several ways to construct reversible networks using reversible gates. The most standard reversible gates are NOT, CNOT and Toffoli gates, which are in general forms of multiple controlled Toffoli gate. Two other gates commonly used in reversible designs are Fredkin and Peres gates. We will present a brief description of these gates next.

Definition 1: A multiple control Toffoli gate has several control lines and a single target line  $x_j$  and this gate maps  $(X_1, X_2, X_3, \dots, X_j, \dots, X_n)$  to  $(X_1, X_2, X_3, \dots, X_{i1}X_{i2}\dots X_{ik} \oplus X_j, \dots, X_n)$  where  $X_{in}$  ( $i=1,2,\dots,k$ ) represent control lines, i.e. the value of the target line is inverted when all control lines are set to 1.

NOT gate is a multiple control Toffoli gate with no controls denoted as TOF ( $X_j$ ). CNOT gate (controlled NOT) is a multiple control Toffoli gate with single control bit which is also known as Feynman gate and denoted as TOF ( $X_i, X_j$ ). The original Toffoli gate is a multiple control gate with two controls denoted as TOF ( $X_{i1}, X_{i2}; X_j$ ). These gates are shown in Figure 2.1.

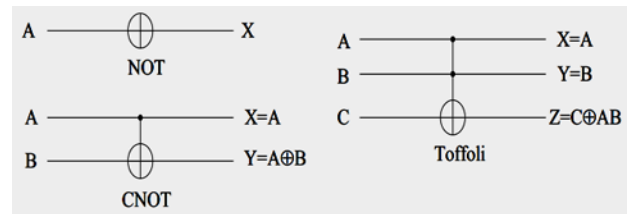


Figure 2.1 Slandered reversible gates.

### III. PREVIOUS WORK

A. Majumder, P. L. Singh, N. Mishra, A. J. Mondal and B. Chowdhury,[1] As the conventional irreversible logic dissipates power for losing bits of information, computing engines has to be designed that do not require energy dissipation but only if computation is done logically reversible. Hence, research on reversible logic has been extensively increased now-a-days for its application in Quantum Computing, nanotechnology, QCA and Low power VLSI etc. In this exploration, we have realized a Quantum Cost efficient Reversible RAM (RRAM) with a new  $3 \times 3$  Reversible Gate named Modified Fredkin (MF). While approaching for RRAM we have also proposed a reversible D Flip-flop with minimum quantum cost (QC), a write enabled reversible master slave D Flip-flop & a  $(i \times 2^i)$  reversible decoder which has outperformed the existing designs in terms of quantum cost, ancilla & garbage outputs. We also have analyzed the architectures in terms of logical depth (worst case delay), hardly addressed in available literature.

L. Gopal, N. S. Mohd Mahayadin, A. K. Chowdhury, A. A. Gopalai and A. K. Singh,[2] In low power circuit design, reversible computing has become one of the most efficient and prominent techniques in recent years. In this exploration, reversible Arithmetic and Logic Unit (ALU) is designed to show its major implications on the Central Processing Unit (CPU). In this exploration, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

S. Nowrin, L. Jamal and H. Tasnim,[3] Power saving circuits are the need of the modern technology which can be achieved by using reversible logic. In this exploration, we propose an efficient design of a reversible  $n \times n$  signed multiplier circuit, where n is the number of bits of each



operand of the multiplier. We propose a novel architecture of a generalized reversible compressor to reduce the number of partial products. Two algorithms have been presented to construct the Partial Product Generation (PPG) circuit and the Multi Operand Addition (MOA) circuit of the proposed multiplier. Our proposed design of MOA circuit needs only two steps to get the final output which is much optimized than existing Wallace Tree multiplier. During the realization process of the multiplier, two new gates have been proposed named as LS gate and LN gate to speed up the generation of partial products. In addition, several theorems on the numbers of gates, garbage outputs, quantum cost of the reversible signed multiplier have been presented to show its efficiency. The comparative study shows that our proposed design is much better than the existing approaches in terms of numbers of gates, garbage outputs, quantum cost and delay. The simulation of the proposed circuit verifies the correctness of the design.

P. S. Phaneendra, C. Vudadha, V. Sreehari and M. B. Srinivas,[5] Reversible computing has emerged as promising technology having its applications in emerging technologies like quantum computing, optical computing etc. This exploration presents a reversible comparator based on prefix tree grouping methodology. The proposed design is realized by cascading three stages. The first stage is a 1-bit reversible comparator which generates 'greater' and 'equal' signals of that operand bit. These signals are combined using prefix tree grouping logic to generate final 'greater' and 'equal' signals. Using these final 'greater' and 'equal' signals, 'lesser' signal is generated in the third stage. The design is optimized in quantum level for efficient performance in all the cost metrics. The proposed 64-bit comparator design results in 14.3% reduced quantum delay, 7.8% reduced quantum cost and 25% reduced garbage outputs when compared with the best existing design of prefix based comparator.

H. M. H. Babu, L. Jamal and N. Saleheen,[4] Reversible logic has captured significant attention in recent time as reducing power consumption is the main concern of digital logic design. It consumes less power by recovering bit loss from its unique input-output mapping. This exploration presents the design of an optimal reversible fault tolerant carry look-ahead adder. We present an algorithm to design a generalized n-bit carry look-ahead adder, where n is the number of bits of the operands. A new technique to calculate the quantum gate complexity of quantum circuits has also been proposed in the exploration. In addition, several theorems on the numbers of garbage outputs, quantum cost, quantum gate complexity and delay of the fault tolerant reversible carry look-ahead adder have been presented to show its optimality. Simulation using Microwind DSCH software has been shown to verify the

correctness of the function of the proposed carry look-ahead adder. The comparative study shows that the proposed design is much better than the existing approach considering all the efficiency parameters of reversible circuit design which includes numbers of gates, quantum cost, delay, quantum gate complexity and garbage outputs. The proposed 8-bit reversible fault tolerant carry look-ahead adder improves 94.9% on the number of gates, 92.4% on the quantum cost, 93.2% on the garbage outputs and 14.5% on the delay than the existing design.

M. Morrison, M. Lewandowski, R. Meana and N. Ranganathan, [6] Reversible logic is an emerging nanotechnology used in the design and implementation of nanotechnology and quantum computing with the main goal of reducing physical entropy gain. Significant work have been produced in the design of fundamental reversible logic structures and arithmetic units, and recent developments in sequential design of reversible circuits has opened new avenues in the implementation of reversible combinational circuits, such as the design and implementation of static (SRAM) and dynamic random-access memory (DRAM). In this exploration, a novel 4\*4 MLMR gate is presented which is used for controlling the read/write logic of a SRAM cell. Next, a reversible SRAM cell is designed and verified. Then, a novel 4\*4 Reversible Decoder (RD) gate, implemented as a 2-to-4 decoder with low delay and cost is presented and verified, and its implementation shown in the construction of a 4x2 reversible SRAM array. Next, a dual-port SRAM cell is presented and verified, and its implementation in a synchronous n-bit reversible dual-port SRAM array is shown. Then, a reversible DRAM cell is presented and verified. The control logic for writing to the DRAM based on Peres gates is shown. The control logic and the DRAM cell are then implemented in a reversible 4x4 DRAM array.

#### IV. PROBLEM STATEMENT

A Reversible RAM may be considered as the brain of any computation and can replace the existing main memory in the forthcoming Quantum devices. The computing power in terms of speed and capacity of today's digital computers has improved tremendously in the last decade. This improvement came mainly due to a revolution in manufacturing technology by developing the ability to manufacture smaller devices and by integrating more devices on a single die. Further development of the current technology will be restricted by physical limits since it won't be possible to shrink devices beyond a certain size. The novel reversible realization and optimization of RRAM will play a big role to reversible logic community to work further for the design of a synchronous N-bit dual-port SRAM array and DRAM array for their application in FPGA or Network-on-chip.

## V. CONCLUSION

The operation of a reversible circuit does not lose information and thus not lose energy. Energy is lost only in reading and initialization. A gate (or circuit) is reversible if it is a one-to-one mapping between sets of input and output values. Thus all output vectors are just permutations of input vectors. Such a circuit can be described by a binary permutation matrix. Reversible circuit is realized using quantum gates such as inverters, Toffoli gates and their special cases - Feynman gates (simple 2\*2 gates). Quantum costs can be calculated when the circuits are designed with smaller primitives such as quantum gates with two inputs and two outputs. Quantum reversible circuit are cost efficient high processing speed and power optimized as compare to classical circuits.

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