A Literature Review on Aging-Aware Reliable Multiplier Design with Adaptive Hold Logic

Deepika Malviya[1], Prof. Deepa Gianchandani[2]

[1]*M-Tech Research Scholar,* [2]*Research Guide*

Department of Electronics & Communication Engineering, SISTec, Bhopal

Abstract: Complementary Metal Oxide Semiconductor (CMOS) has become the dominant technology in the electronic industry for the past several decades, and it is expected to stay in such position for the next years. Before the end of 2003, microprocessors were able to produce 90 nm processes, and now production on 45 nm and below is coming out. However, the scaling of CMOS technology into deep submicron regimes has brought about new reliability challenges in MOSFET device such as hot carrier Injection (HCI), Negative Bias Temperature Instability (NBTI) [1,2], Time Dependent Dielectric Breakdown (TDDB), radiation induced damage, etc., which can pose a limit to the device scaling, and cause circuit performance degradation. When integrate circuits work for long time, especially for today's CMOS technology, heat of chips will increase significantly. For this reason, one of the dominant reliability issues - Negative Bias Temperature Instability (NBTI) in PMOS transistors.

Keywords - Adaptive Hold Logic, Aging Effect, Multiplier.

I. INTRODUCTION

The search for high dielectric constant (high-for near-future gate dielectrics in MOS ULSI a device is) materials currently an enormous materials and technological challenge. Most of the current research and development activities in high dielectrics are concentrated on binary metal oxides and silicates. As the conventional SiO_2/ SiO_xN_y gate dielectric film is scaled, gate leakage current density increases significantly and has become an important scaling limitation. This increase in gate leakage current density with scaling is the main motivation for replacing the conventional SiO_2-based gate dielectrics with higher films. In terms of gate leakage, high materials offer significant (typically 2–6 orders of magnitude) leakage current reduction due to increased physical thickness of the stack which has recently been demonstrated by many research groups. While HfO_2-based (and other high-candidates) show a desired effect of significantly reduced gate tunnelling (leakage) current, there are still a number of fundamental issues, such as fixed charge, reduced channel mobility and trapped charge, which have to be understood and solved for successful high- integration into the silicon CMOS technology [6].

During NBTI–induced device degradation, the holes in the inversion layer react with the hydrogen-silicon bonds (Si-H) at the Si/SiO2 interface and then release the hydrogen species (atom, molecule or ion) by breaking the Si–H bonds, because the two-electron Si-H covalent bond is weakened. Once a hole is captured and this weakened bond is easily broken at relatively moderate temperature.

MOSFETs have been the major force behind the tremendous development in the microelectronics industry, yielding unprecedented scientific and technological advancements. This fundamental impact of MOSFETs has been facilitated by the phenomenal properties of both Si and its oxide, SiO2. The ability to integrate various circuit components on the same substrate and the scalability of the dimensions of the MOSFETs have allowed increasing density of transistors with higher speed and computational capability along with lower power consumption and cost per MOSFET.

The progress in MOSFET based microelectronics has not been without its problems. The operating requirements of ICs put stress on the devices, leading to performance and reliability problems. MOSFETs, and particularly the oxide, degrade during the device operation and cannot retain its original specifications. One general degradation type is defect generation in the oxide bulk or at the Si-SiO2 interface over time. The defects can increase leakage current through the gate dielectric, change transistor metrics such as the threshold voltage or result in the device failure due to oxide breakdown.

N ANOSCALE SRAM design must ensure robust operations against large leakage, PVT variation, and degradation over the usage lifetime. The negative-bias temperature instability (NBTI) has long been known to be a serious concern for scaled PFET. With the introduction of high-k metal gate device and its associated charge-trapping related threshold voltage instability, the positive-bias

temperature instability (PBTI) has become more significant in NFET [1], [2]. The NBTI and PBTI effects cause the threshold voltage of transistors to drift with stress time, thus weakening PFET and NFET respectively.

SRAM design composes of logic control circuits and bit cells. Logic control circuits include decoders and Read/Write access timing control circuits. In order to trace real word-line and bit line delay, and Write-time of bit cells, replica circuits are often used in SRAM timing control circuit. With serious transistors' geometry/dimension variations and intrinsic fluctuations, the mismatch is more serious in SRAM bit cells. Monte Carlo simulations and statistical methods are needed to design a robust bit cell. With the drifts induced by NBTI and PBTI, and mismatches among individual cell transistors become more serious, leading to degradation of stability and the already poor design margin. The Read latency of a bit cell is more sensitive to PBTI and increases with stress time, whereas the Write margin (WM) may improve or degrade depending on the signal (stress) probability of the bit cell. Of bit cells has also been shown to degrade with time. Furthermore, the design of SRAM logic control circuit should also consider the variation and leakage effect in order to improve SRAM access failure rate. These circuits are also under NBTI and PBTI stress. It leads to drifts of trip points of logic circuits and degradation of signal propagation delays. The drifts of trip points and degradation of propagation delays depend on the input pattern. As a result, timing mismatch between bit cells and SRAM logic control circuits occurs, leading to access performance degradation and unreliable access operations.

a. NBTI Time-dependence

The characterization period of the transistor degradation is very short compared to the desired lifetime (e.g., few weeks for the former, about 10 years for the latter) of a transistor. For a given technology generation, accelerated characterization tests with higher voltages and temperatures with respect to the operating conditions are performed, the characteristic NBTI time-dependence is extracted, and the results are projected to the long device lifetimes. In practise, accurate quantification of the degradation is of great interest because the lifetimes of the MOSFETs or circuits are directly related to the time-dependence of damage.

Moreover, the NBTI degradation under the accelerated test conditions and the real operating conditions can vary. Therefore, robust, physics-based, and well-calibrated models are needed to capture these aspects of NBTI for present and future-generation devices and stress conditions.

The NBTI time-dependence is explored by encapsulating the physical mechanisms into a phenomenological framework, i.e., Reaction-Diffusion (R-D) model. Although several models have been proposed for the time-dependence of NBTI, the R-D provides a very robust framework to explain experimental observations.

The model is based on interface trap generation and related hydrogen dynamics [42]. The generation takes place at the semiconductor/oxide interface which is a rough surface where the highly ordered crystalline channel and the amorphous SiO_2 dielectric meet. At the junction of these dissimilar materials, some of the Si atoms from the channel remain dangling without satisfied chemical bonds, thus, forming the interface traps. The traps lead to poor device performance; therefore the transistors are annealed in hydrogen ambient during the manufacture.

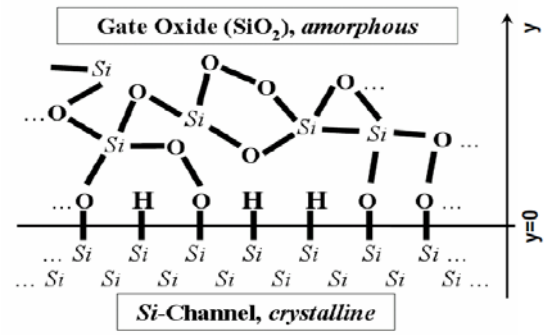

Fig.1. the schematic of the Si/oxide interface of a MOSFET.

b. Saturation behaviour

The NBTI literature until late 1990s generally characterized the interface trap (NIT) generation as a function of time, (t), as a power-law (i.e., $N_{IT} \alpha t^n$) with $n \tilde{=} 0.3-0.5$. This value of n was assumed robust, that is, independent of stress time. This time-independent exponent had been the unique signature of NBTI degradation and traditional theoretical models of NBTI strived to interpret the constancy of *n* satisfactorily.

It became increasingly clear in late 1990s, as the semiconductor industry began to struggle with NBTI issue, that the projected IC lifetime based on $n \approx 0.30-0.50$ will be unacceptable. This led to an intense re-examination of the NBTI time-exponent. The essence of many measurements of n done since late 1990s is the following: $n \approx 0.3 - 0.5$ at the early stage of degradation, however at long stress times, *n* gradually decreased to $\approx 0.12 - 0.15$. This is good news for semiconductor industry because lower exponents translate to longer extrapolated lifetime for CMOS circuits. However, this time-dependent change in n (in other words, quasi-saturation of trap generation) poses a challenge to old theories of NBTI which focused on the

interpretation of time-independent exponents. The old NBTI theories had to be generalized to explain the new phenomena and establish appropriate voltage and temperature scaling laws. Five different mechanisms for NBTI quasi-saturation have been proposed: a) Reflection of H at the poly/oxide interface, b) Breaking of all Si − H bonds at the Si/SiO2 interface, c) Variation of bonding strength of the precursors. d) Transition from atomic to molecular hydrogen and e) Artifact of finite measurement delay. All these models are based on various refinements of basic Reaction-Diffusion (R-D) model.

The 2005 ITRS projects the scaling of CMOS technology to 32nm and 22nm nodes in ten years, with equivalent oxide thickness as thin as 5A. In the nanometer regime, physical factors that previously had little impact on circuit performance are now becoming increasingly significant. This is especially true for variability and reliability concerns that require careful attention during the design stage. In particular, there has been a recent escalation in interest on the reliability impact of PMOS negative bias temperature instability (NBTI). NBTI occurs under negative gate voltage (e.g., V_{gs}= -V_{DD}) and is measured as an increase in the magnitude of threshold voltage. It mostly affects the PMOS transistor and degrades the device drive current, circuit speed, noise margin, and the matching property. Indeed, as gate oxide gets thinner than 4nm, the threshold voltage change caused by NBTI for the PMOS transistor has become the dominant factor to limit the life time, which is much shorter than that defined by hot-carrier induced degradation (HCI) of the NMOS transistor [2]. Furthermore, different from HCI that occurs only during dynamic switching, NBTI is caused during static stress on the oxide even without current flow. Consequently, the situation of the NBTI degradation is exacerbated in the nanoscale design as advanced digital systems tend to have longer standby time for lower power consumption. As the NBTI effect becomes more severe with continuous scaling, it is critical to understand, simulate, and minimize the impact of NBTI in the early design stage to ensure the reliable operation of circuits for a desired period of time.

To date, research works on NBTI have been active only within the communities of device and reliability physics. Partly due to its complexity and emerging status, design knowledge and CAD tools for managing the NBTI degradation are not widely available [1,6]. Leading industrial companies do develop their own models and tools to handle this effect. These tools, however, are usually proprietary and empirical to a specific technology. In this case, a more general and SPICE compatible model that can accurately predict the degradation would be very useful. This predictive model will further serve as a cornerstone to circuit design and optimization in the presence of the NBTI degradation.

II. LITERATURE SURVEY

C. Lin, Y. H. Cho and Y. M. Yang,[1] Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = -Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column or row-bypassing multiplier. The experimental results show that our proposed architecture with 16 × 16 and 32 × 32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column-bypassing multipliers. Furthermore, our proposed architecture with 16 × 16 and 32 × 32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement as compared with 16×16 and 32 × 32 fixed-latency row-bypassing multipliers.

S. Zafar et al., [2] Threshold voltage (Vt) of a field effect transistor (FET) is observed to shift with stressing time and this stress induced V t shift is an important transistor reliability issue. Vt shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping. In this paper, we present a comparative study of NBTI and PBTI for a variety of FETs with different dielectric stacks and gate materials. The study has two parts. In part I, NBTI and PBTI measurements are performed for FUSI NiSi gated FETs with SiO2 SiO2/HfO2 and SiO2/HfSiO as gate dielectric stacks and the results are compared with those for conventional SiON/poly-Si FETs. The main results are: (i) NBTI for SiO 2/NiSi and SiO2/HfO2/NiSi are same as those conventional SiON/poly-Si FETs; (ii) PBTI significantly increases as the Hf content in the high K layer is increased; and (iii) PBTI is a greater reliability issue than NBTI for HfO2/NiSi FETs. In part II of the study, NBTI and PBTI measurements are performed for SiO2/HfO2 devices with TiN and Re as gates and the results are compared with those for NiSi gated FETs. The main results

are: (i) NBTI for SiO 2/HfO2/TiN and SiO2/HfO2/Re pFETs are similar with those observed for NiSi gated pFETs; and (ii) PBTI in TiN and Re gated HfO2 devices is much smaller than those observed for SiO2/HfO2/NiSi. In summary for SiO2/HfO2 stacks, NBTI is observed to be independent of gate material whereas PBTI is significantly worse for FUSI gated devices. Consequently, HfO2 FETs with TiN and Re gates exhibit over all superior transistor reliability characteristics in comparison to HfO2/FUSI FETs

S. Zafar, A. Kumar, E. Gusev and E. Cartier, [3] Over recent years, there has been increasing research and development efforts to replace SiO2 with high dielectric constant (high-κ) materials such as HfO2, HfSiO, and Al2O3. An important transistor reliability issue is the threshold voltage stability under prolonged stressing. In these materials, threshold voltage is observed to shift with stressing time and conditions, thereby giving rise to threshold voltage instabilities. In this paper, we review various causes of threshold voltage instability: charge trapping under positive bias stressing, positive charge creation under negative bias stressing (NBTI), hot-carrier stressing, de-trapping and transient charge trapping effects in high-κ gate dielectric stacks. Experimental and modeling studies for these threshold voltage instabilities are reviewed.

H. I. Yang, S. C. Yang, W. Hwang and C. T. Chuang [4] Negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) weaken PFET and NFET over the lifetime of usage, leading to performance and reliability degradation of nanoscale CMOS SRAM. In addition, most of the state-of-the-art SRAM designs employ replica timing control circuit to mitigate the effects of leakage and process variation, optimize the performance, and reduce power consumption. NBTI and PBTI also degrade the timing control circuits and may render them ineffective. In this paper, we provide comprehensive analyses on the impacts of NBTI and PBTI on a two-port 8T SRAM design, including the stability and Write margin of the cell, Read/Write access paths, and replica timing control circuits. We show, for the first time, that because the Read/Write replica timing control circuits are activated in every Read/Write cycle, they exhibit distinctively different degradation behavior from the normal array access paths, resulting in degradation of timing control and performance. We also discuss degradation tolerant design techniques to mitigate the performance and reliability degradation induced by NBTI/PBTI.

R. Vattikonda, Wenping Wang and Yu Cao [5] Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this paper, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robust design solutions: (1) the most effective techniques to mitigate the NBTI degradation are VDD tuning, PMOS sizing, and reducing the duty cycle; (2) an optimal VDD exists to minimize the degradation of circuit performance; (3) tuning gate length or the switching frequency has little impact on the NBTI effect; (4) a new switching scenario is identified for worst case timing analysis during NBTI stress

S. V. Kumar, C. H. Kim and S. S. Sapatnekar, [6] Negative bias temperature instability (NBTI) in PMOS transistors has become a major reliability concern in nanometer scale design, causing the temporal degradation of the threshold voltage of the PMOS transistors, and the delay of digital circuits. A novel method to characterize the delay of every gate in the standard cell library, as a function of the signal probability of each of its inputs, is developed. Accordingly, a technology mapping technique that incorporates the NBTI stress and recovery effects, in order to ensure optimal performance of the circuit, during its entire lifetime, is presented. Our technique, demonstrated over 65 nm benchmarks shows an average of 10 % area recovery, and 12 % power savings, as against a pessimistic method that assumes constant stress on all PMOS transistors in the design.

III. PROBLEM IDENTIFICATION

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that our proposed architecture with 16×16 and 32×32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement compared with the 16 × 16 and 32 × 32 FLCB multipliers, respectively. Furthermore, our proposed architecture with the 16×16 and 32×32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement compared with the 16 × 16 and 32 × 32 FLRB multipliers. In addition, the variable-latency bypassing multipliers exhibited the lowest average EDP and achieved up to 10.45% EDP reduction in 32 × 32 VLCB multipliers. Note that in addition to the BTI effect that increases transistor delay, interconnect also has its aging issue, which is called electromigration. Electromigration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the

wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electromigration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electromigration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electromigration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period.

IV. CONCLUSION

Negative-bias temperature instability (NBTI) is a main reliability issue in MOSFETs. The NBTI effect is more seen in a p-channel MOSFET when stressed with negative gate voltages at elevated temperatures. The NBTI causes the absolute value of threshold voltage to increase and consequent decrease in drain current and decrease of other important parameters like trans-conductance, channel mobility of a MOSFET. The same effects can be seen in n-channel MOSFET's too but the degradation is very less compared to that of a p-channel MOSFET. Therefore it is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage like in an inverter and ring oscillator.

REFRENCES

[1] I. C. Lin, Y. H. Cho and Y. M. Yang, "Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 3, pp. 544-556, March 2015.

[2] S. Zafar et al., "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO2/HfO2 Stacks with FUSI, TiN, Re Gates," VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on, Honolulu, HI, 2006, pp. 23-25.

[3] S. Zafar, A. Kumar, E. Gusev and E. Cartier, "Threshold voltage instabilities in high-κ gate dielectric stacks," in IEEE Transactions on Device and Materials Reliability, vol. 5, no. 1, pp. 45-64, March 2005.

[4] H. I. Yang, S. C. Yang, W. Hwang and C. T. Chuang, "Impacts of NBTI/PBTI on Timing Control Circuits and Degradation Tolerant Design in Nanoscale CMOS SRAM," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 6, pp. 1239-1251, June 2011.

[5] R. Vattikonda, Wenping Wang and Yu Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," Design Automation Conference, 2006 43rd ACM/IEEE, San Francisco, CA, 2006,

[6] S. V. Kumar, C. H. Kim and S. S. Sapatnekar, "NBTI-Aware Synthesis of Digital Circuits," Design Automation Conference, 2007. DAC '07. 44th ACM/IEEE, San Diego, CA, 2007, pp. 370-375.