

# A Review on a Novel Delay & Quantum Cost Efficient Reversible Realization of RAM

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**Abstract** - Programmable reversible logic is emerging as a prospective design style for Arithmetic operations lie at the foundation of modern nanotechnology and quantum computing. Improvements to arithmetic circuits can result in improvements to the entire computing system. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. A garbage-free reversible computing system it is especially important that the arithmetic circuits are also garbage-free, but how to do this is not always obvious, and history shows that rethinking our current knowledge can be necessary. There are three basic 2x2 reversible logic gates. The Controlled-Not gate - commonly called the Feynman gate - is designed to produce the following output states:  $P = A$  and  $Q = A \oplus B$ . Since fanout is expressively forbidden in reversible logic, since a fanout has one input and two outputs, the Feynman gate may be used to duplicate a signal when  $B$  is equal to 0. Gates utilize the unitary operators to produce reversible logic calculations when a select line is set at '1'. In these work an extensive study and analysis of the reversible logic has reviewed.

**Keywords**- Arithmetic operations, Reversible logics, Quantum Cost Efficient, Reversible logic gates.

## I. INTRODUCTION

The need and importance of quantum circuits in the area of quantum computing was first realized by Feynman in 1982 where he had shown that quantum mechanical systems cannot be efficiently simulated in a classical computer. Later in 1985 David Deutch had proposed a design of universal quantum Turing machine and provided an algorithm which proved that quantum computer can solve certain problems faster than their classical counterpart. The legacy continued for the last 25 years and in the domain of quantum computing several new possibilities appeared which are impossible in classical domain. To be precise, quantum teleportation, infinitesimally secured cryptography and super dense-coding do not have any classical analogue. Again all these unique features of quantum communication are associated with quantum circuits. In other words, we require quantum circuits to implement quantum algorithms and protocols. Thus the clear understanding of quantum circuits is important for the development of quantum computing.

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation.

Since ancient times, humanity has been seeking tools to help us perform tasks which involve calculations. Such are computing the area of a land, computing the stresses on rods in bridges, or finding the shortest route from one place to another. A common feature of all these tasks is their structure:

*Input* ---> *Computation* ---> *Output*

The computation part of the process is inevitably performed by a dynamical physical system, evolving in time. In this sense, the question of what can be computed is intermingled with the physical question of which systems can be physically realized. If one wants to perform a certain computation task, one should seek the appropriate physical system, such that the evolution in time of the system corresponds to the desired computation process. If such a system is initialized according to the input, its final state will correspond to the desired output. These facts have motivated to do the present work in which studied different perspectives of synthesis, optimization and testing of reversible and quantum circuits.

## II. REVERSIBLE CIRCUIT MODEL

Reversible circuit is composed of reversible logic gates. The logic gates used in conventional circuit or digital

designing is irreversible (except IDENTITY and NOT gate) that means that the input cannot be traced from output. For example, the AND gate, OR gate, NAND gate etc. are irreversible gates.

A reversible circuit is represented by network of wires that carry bit values to gates that perform elementary operations on the bits. The wires are referred to as bit lines. The input bits are written on the left side of the circuit and the output bits are written on the right side of the circuit. The circuit is acyclic i.e. it is linear and time in circuit propagates from left to right. At every time step each wire

can enter at most one gate, The target appear as  $\oplus$  and control appear as  $\bullet$  on the bit line also called wire which are horizontal lines that carry the bit. The state of the bit can be 0 or 1. figure 2.1 illustrated a reversible circuit. The first bit line and second bit line are the input bits while the third bit line is a constant input (extra bit added to achieve reversibility) with input value 0. At the output the first and second bit line are garbage outputs which are no longer required for computation and the third bit line gives the desired output. A considerable amount of interesting work has already been reported in the field of synthesis, optimization, evaluation and testing of reversible circuits.

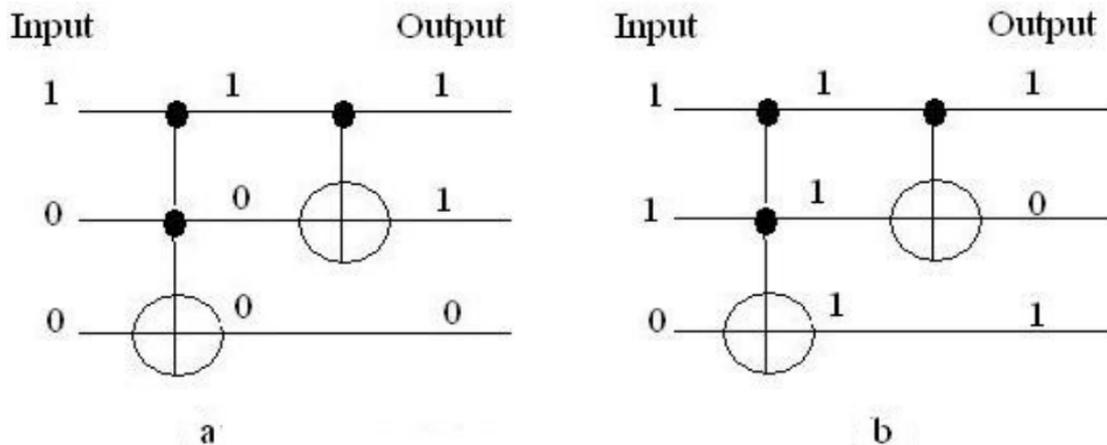


Figure 2.1 Typical Reversible circuit of a Half Adder.

### A. Basic Idea of Quantum

To understand quantum circuits first need to understand the meaning of a qubit and how it differs from a bit. The Physics of quantum computing is quantum mechanics and take the liberty to choose the linear algebra model or the Dirac notation. Dirac's notation is known as *bra – ket* notation. In this notation a state vector is written as  $|\psi\rangle$  which is pronounced as ket  $\psi$ . The dual of this state is the conjugate of the state vector  $\psi$  and is denoted as  $\langle\psi|$  which is pronounced as bra  $\psi$ . In this notation the quantum states are represented by vectors in a complex finite dimensional vector space called inner product space) Hilbert space. A quantum gate is a unitary operation performed on a quantum system. A one-qubit gate is any unitary operation on a 2 dimensional quantum system (i.e. on a qubit).

### B. Gate Count (circuit cost)

Gate count is the total number of gates in a circuit. It is a quantitative measure of quality of a circuit and often referred as circuit cost. It is not unique. If one is allowed to introduce a new gate or if a complex gate library is used then the gate count can be considerably reduced. For example, let us consider the Half Adder circuit shown in Figure 2.1. It is implemented using 2 gates therefore its gate count is 2. Now we can put the two gates in a box and

consider the box as a new gate. The gate count in that situation is 1. It is important to understand that each reversible gate is represented by a unitary matrix, the new gate will have a new unitary matrix formed from matrix multiplication of CCnot and Cnot therefore this new gate will solely perform as a reversible Half Adder under special condition that it's third bit value remains 0. Thus if one is allowed to introduce a new gate or a complex gate library then the gate count can be considerably reduced. This may be clearly understood for quantum gate perspective since reversible gate is only a special case of quantum gate.

### C. Garbage Bits

Garbage bits are the additional output that makes a function reversible and is not used for further computations. Since the garbage bits are not used for further computation hence large number of garbage bits is not desirable in a reversible circuit. In a reversible function, if  $q$  be the maximum number of times an output pattern is repeated then minimum number of garbage bits required to ensure reversibility is  $\log_2(q)$ .

### D. Quantum Cost

The quantum cost of a reversible gate is the number of elementary quantum gates needed to implement the gate.

Elementary quantum gates are the elementary building block, like Not gate, Cnot gate, Controlled-V, Controlled-V + Rotation gates etc. Actually all (1 x 1) and (2 x 2) gates are considered as elementary quantum gates and the cost of all elementary quantum gates are considered as one.

#### E. Transistor Cost

In CMOS technology the reversible gates can be realized by transistors. The transistor cost ( $TrC$ ) of a  $TOFn$  is given by  $8.n$  where  $n$  is the number and that of Cnot gate is 8.  $TrC$  for generalized Fredkin gate is  $8 * (n + 1)$  where  $n$  is number of control lines. Thus the  $TrC$  of usual Fredkin gate is 16.

#### F. Total cost

A circuit is considered better than another circuit (designed for the same computational task) if it has lesser number of garbage bits, circuit cost and quantum cost. But it is often observed that reduction of circuit cost leads to increase in garbage bits and reduction of quantum cost leads to increase in circuit cost. Keeping these in mind we have introduced a new parameter called Total cost (TC) which is the sum of gate count of an optimized circuit, number of garbage bits and quantum cost.

#### G. Delay

Delay is considered as an important measure to evaluate a logic design. Kaye has defined that a reversible circuit design can be visualized as a sequence of discrete time slices and depth is summation of total time slices. Mohammadi and Eshghi have reported that delay is directly proportional to depth. Interestingly, Maslov et al. has prescribed a level compaction algorithm to optimize the depth of a circuit (level compaction). The protocol provides minimal delay.

### III. PRIOR WORK

A. Majumder, P. L. Singh, N. Mishra, A. J. Mondal and B. Chowdhury,[1] As the conventional irreversible logic dissipates power for losing bits of information, computing engines has to be designed that do not require energy dissipation but only if computation is done logically reversible. Hence, research on reversible logic has been extensively increased now-a-days for its application in Quantum Computing, nanotechnology; QCA and Low power VLSI etc. In this research work, we have realized a Quantum Cost efficient Reversible RAM (RRAM) with a new  $3 \times 3$  Reversible Gate named Modified Fredkin (MF). While approaching for RRAM we have also proposed a reversible D Flip-flop with minimum quantum cost (QC), a write enabled reversible master slave D Flip-flop & a ( $i \times$

$2^i$ ) reversible decoder which has outperformed the existing designs in terms of quantum cost, ancilla & garbage outputs. We also have analyzed the architectures in terms of logical depth (worst case delay), hardly addressed in available literature.

S. Nowrin, L. Jamal and H. Tasnim,[2] Power saving circuits are the need of the modern technology which can be achieved by using reversible logic. In this research work, we propose an efficient design of a reversible  $n \times n$  signed multiplier circuit, where  $n$  is the number of bits of each operand of the multiplier. We propose a novel architecture of a generalized reversible compressor to reduce the number of partial products. Two algorithms have been presented to construct the Partial Product Generation (PPG) circuit and the Multi Operand Addition (MOA) circuit of the proposed multiplier. Our proposed design of MOA circuit needs only two steps to get the final output which is much optimized than existing Wallace Tree multiplier. During the realization process of the multiplier, two new gates have been proposed named as LS gate and LN gate to speed up the generation of partial products. In addition, several theorems on the numbers of gates, garbage outputs, and quantum cost of the reversible signed multiplier have been presented to show its efficiency. The comparative study shows that our proposed design is much better than the existing approaches in terms of numbers of gates, garbage outputs, quantum cost and delay. The simulation of the proposed circuit verifies the correctness of the design.

L. Gopal, N. S. Mohd Mahayadin, A. K. Chowdhury, A. A. Gopalai and A. K. Singh,[3] In low power circuit design, reversible computing has become one of the most efficient and prominent techniques in recent years. In this research work, reversible Arithmetic and Logic Unit (ALU) is designed to show its major implications on the Central Processing Unit (CPU). In this research work, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

P. S. Phaneendra, C. Vudadha, V. Sreehari and M. B. Srinivas,[4] Reversible computing has emerged as promising technology having its applications in emerging

technologies like quantum computing, optical computing etc. This research work presents a reversible comparator based on prefix tree grouping methodology. The proposed design is realized by cascading three stages. The first stage is a 1-bit reversible comparator which generates 'greater' and 'equal' signals of that operand bit. These signals are combined using prefix tree grouping logic to generate final 'greater' and 'equal' signals. Using these final 'greater' and 'equal' signals, 'lesser' signal is generated in the third stage. The design is optimized in quantum level for efficient performance in all the cost metrics. The proposed 64-bit comparator design results in 14.3% reduced quantum delay, 7.8% reduced quantum cost and 25% reduced garbage outputs when compared with the best existing design of prefix based comparator.

H. M. H. Babu, L. Jamal and N. Saleheen,[5] Reversible logic has captured significant attention in recent time as reducing power consumption is the main concern of digital logic design. It consumes less power by recovering bit loss from its unique input-output mapping. This research work presents the design of an optimal reversible fault tolerant carry look-ahead adder. We present an algorithm to design a generalized n-bit carry look-ahead adder, where n is the number of bits of the operands. A new technique to calculate the quantum gate complexity of quantum circuits has also been proposed in the research work. In addition, several theorems on the numbers of garbage outputs, quantum cost, quantum gate complexity and delay of the fault tolerant reversible carry look-ahead adder have been presented to show its optimality. Simulation using Microwind DSCH software has been shown to verify the correctness of the function of the proposed carry look-ahead adder. The comparative study shows that the proposed design is much better than the existing approach considering all the efficiency parameters of reversible circuit design which includes numbers of gates, quantum cost, delay, quantum gate complexity and garbage outputs. The proposed 8-bit reversible fault tolerant carry look-ahead adder improves 94.9% on the number of gates, 92.4% on the quantum cost, 93.2% on the garbage outputs and 14.5% on the delay than the existing design.

M. Morrison, M. Lewandowski, R. Meana and N. Ranganathan,[6] Reversible logic is an emerging nanotechnology used in the design and implementation of nanotechnology and quantum computing with the main goal of reducing physical entropy gain. Significant work have been produced in the design of fundamental reversible logic structures and arithmetic units, and recent developments in sequential design of reversible circuits has opened new avenues in the implementation of reversible combinational circuits, such as the design and implementation of static (SRAM) and dynamic random-

access memory (DRAM). In this research work, a novel 4\*4 MLMR gate is presented which is used for controlling the read/write logic of a SRAM cell. Next, a reversible SRAM cell is designed and verified. Then, a novel 4\*4 Reversible Decoder (RD) gate, implemented as a 2-to-4 decoder with low delay and cost is presented and verified, and its implementation shown in the construction of a 4x2 reversible SRAM array. Next, a dual-port SRAM cell is presented and verified, and its implementation in a synchronous n-bit reversible dual-port SRAM array is shown. Then, a reversible DRAM cell is presented and verified. The control logic for writing to the DRAM based on Peres gates is shown. The control logic and the DRAM cell are then implemented in a reversible 4x4 DRAM array.

#### IV. PROBLEM STATEMENT

A Reversible RAM may be considered as the brain of any computation and can replace the existing main memory in the forthcoming Quantum devices. In past work, [1] a quantum cost efficient novel architecture of RRAM with the help of proposed MF gate, Reversible D-FF and decoder. Proper algorithms and lemmas have been mentioned for clarification of proposed design so as to have some idea about their efficiency. Optimization of RRAM will play a big role to reversible logic community to work further for the design of a synchronous N-bit dual-port SRAM array and DRAM array for their application in FPGA or Network-on-chip.

#### V. CONCLUSION

Throughout the brief study and The basic principle of reversible computing is that a objective device with an identical number of input and output lines will produce a computing environment where the electrostatics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. it may can be summarized that quantum reversible circuit has brought a revolution in semiconductor industries for better performance high speed and cost effective. There are lots of work has done in the field of reversible gates and quantum cost efficient circuit and still it need more time and effort.

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