Low Power Dissipation 12 Bit Pipe Line Analog To Digital Converter Using 0.18 µm Technology

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Abstract - Analog-to-digital converters (ADCs) are basic design blocks and are currently adopted in many application fields to get better digital systems, which accomplish superior performances with respect to analog solutions. With the fast advancement of CMOS fabrication technology, further signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and high re-configurability. This paper illustrate a 12 bit 75-Msample/s analog-to-digital converter fabricated in a0.18-um CMOS technology. The converter uses pipelined six stage and implement 2 bit per stage.

Key word: Flash ADC, Pipe Line ADC, Amplifier.

I INTRODUCTION

Pipeline analog-to-digital converters (ADCS) represent the majority of the ADC market for medium-to high resolution ADCS. Pipeline ADCS provide up to 5 Msps sampling rates with resolutions from 8 to 18 bits. The Pipeline ADC architecture allows for high performance, low power ADCS to be packaged in small form factors for today's applications. With ADC we have designed 4 bit low power high speed Pipeline ADC with 0.18µm technology. like IC fabrication technology has advanced, more

Analog signal processing functions have been replaced by digital blocks. Analog-to-digital converters (ADCs) retain an important role in most modern electronic systems because most signals of interest are analog in nature and must to

Be converted to digital signals for further signal processing in the digital domain. There is wide Variety of different ADC architectures available depending on the requirements of the application.

Pipeline ADCs are one of the best examples. It typically generate one bit per clock cycle, the Benefits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges.[14] The pipeline analog-to-digital converter (ADC) is a promising topology for high-speed data conversion with compact area and efficient power dissipation. [15][18][10]

Pipelined ADCs are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, studio cameras, ultrasound monitors, and many other high speed applications. [12][22]

The Pipeline ADC implemented in this approach is a dynamic approach that combines the ease of a flash with the residue type operation for pipeline implementation. Many novel ideas have been implementing to improve the architecture such as fore-front and backdrop calibration [6][7][8].

This study is arranged as section II contains mythology. The single stage of pipe line ADC is described in section III. Section IV represents the simulation and Experimental results are shown in this section .it is shows various wave form of sub module of single stage pipe line ADC .V represent the comparison result of pipeline design in term of various parameter. Section .VI represents conclusion and discussions. VII references.

II MYTHOLOGY

The design was fabricated using 0.18 µm CMOS technology and the design is implemented in TSMC 0.18µm CMOS technology. Internal flash ADC is 3-bit per stage used which increases the comparator size, thereby increasing the circuit complexity because flash ADC[8] consists of a 2^{n-1} to comparators. Since resolution increases with the comparators size, this pipelined ADC architectures were studied in proposed work. In this work, a 2-bit internal flash is used and resolution & gain have been enhanced.

The main objective to design 12 nit pipe line analog to digital converter where each stage consists of two bits and total six stages required to get output of 12 bit.

III SINGLE STAGES ADC DESIGN

As the through put should be as fast as of flash ADC, each stage of the pipeline ADC is inherited form flash structural design. The resolution of each one step will choose how many comparators are set, what will be the latency of the structure This is the motivation, which will simplify the design of other sub-blocks of each stage, For the design of each stage of pipeline ADC), the required components are. Show in fig.1

- Sample and Hold.
- TIQ Comparator.
- 2-bit DAC.

- Amplifier configure for gain of 4.
- Analog Adder.
- Operational amplifier [13]

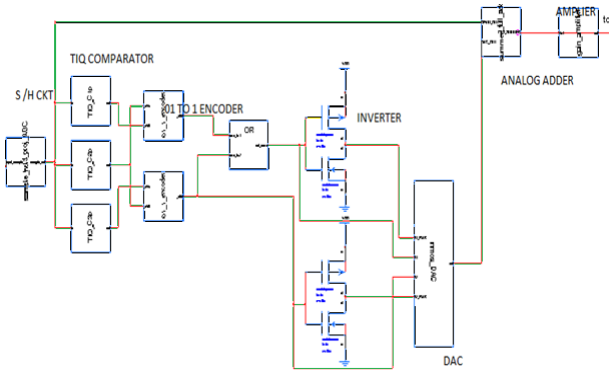

Fig.1 single stage pipeline ADC architecture

- **Design of Comparator**

Implemented flash ADC features the Threshold Inverter Quantization (TIQ) [25] technique for high Speed and low power ADC using standard CMOS technology this design also save the require of reference generator and the comparator will much quicker than the conventional comparator because

it require only 4 transistors (first one to locate the requisite threshold voltage and next one to get requisite gain and avert unbalanced propagation impediment). show in fig.2 Mathematically the value of threshold voltage is govern by means of mathematically term

$$V_t = \frac{r(V_{dd}-V_{tp})+V_{tn}}{1+r} \qquad r = \sqrt{\frac{K_p}{K_n}}$$

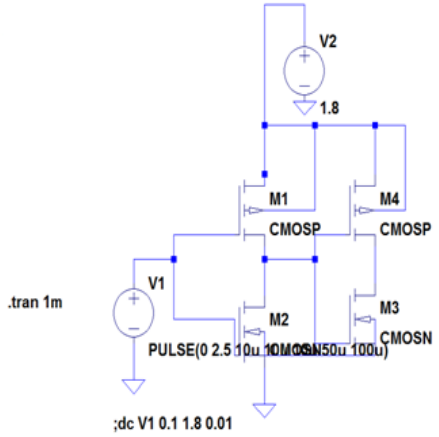

Fig.2 comparator circuit

- **Sample and hold**

Sample and hold circuits are used to sample an analog signal and to store its value for some length of time (for digital code conversion).[21][24] It is heavily used in data converters. Sample-and-hold is also referred to as track-and-hold circuits. Once the signal has been tracked, the ADC throws a switch to disconnect the input signal from the front end; it then holds that input signal level long Enough for the ADC to complete its conversion cycle The switch and hold capacitors must charge up and hold the signal representation for considerable times to allow the ADC quantizer to accurately estimate the changing input signal amplitude. Show in fig.3

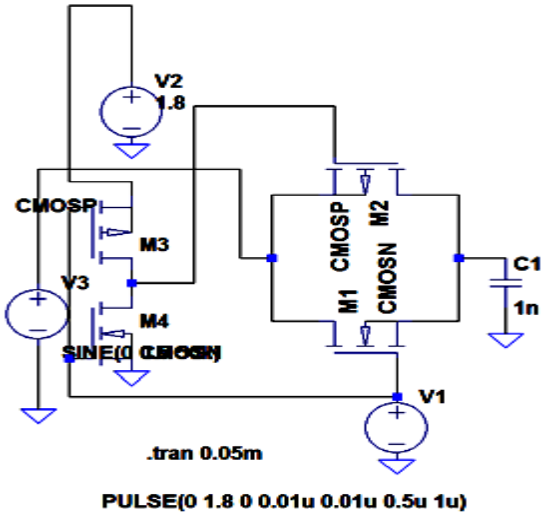

Fig. 3 sample and hold circuit

- **TC To BC Encoder**

The thermometer code-to-binary code encoder has become the bottleneck of the ultra-high speed flash ADCs. Thermometer code to-binary code encoder that is highly suitable for the ultrahigh speed flash ADCs A flash analog-to-digital converter (ADC) is known for its high speed operation. An n bit ADC's front-end consists of N 1 (where N = 2n) voltage comparators, comparing fully parallel the incoming analog signal with N 1 reference voltages. The comparators produce the digital thermometer-code (TC),[12][11] and the remaining back-end of a flash ADC consists of a thermometer code-to-binary code encoder, as shown in Figure 4

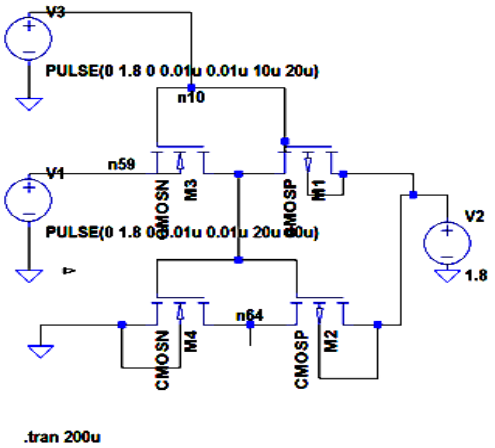

Fig.4 TC to BC converter circuit

- **Design of Inverting Gain Amplifier**

Each pipeline ADC stage have one gain block, whose gain depends on the number of output bits of each stage, Mathematically –

$Av = 2^n$

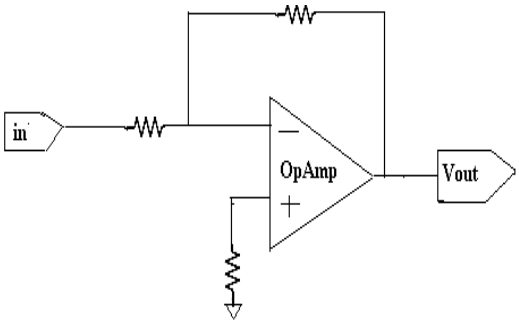

Figure 5 Inverting Gain Amplifier Configured For Gain Of 4

Where Av is the gain of amplifier and n is the number of bits of each stage. Thus the [19] OPAMP has to be configured in closed loop style, since, the proposed design has only one bit per stage, and thus the required gain is 4. The configuration is shown in figure 5

- **Design of D Flip-Flop**

It is one of the necessary elements in the pipeline ADC, the main point to raise here is that, it is used as delay element which will synchronize the bits of the all stages, by configuring the flip-flop as varying length shift register, it will synchronize the output of pipeline ADC.

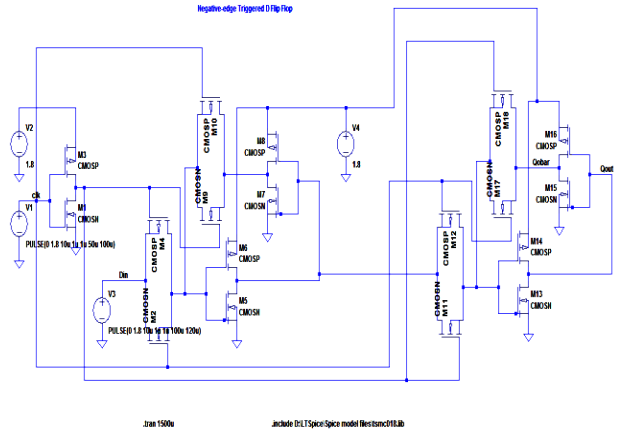

Fig.6 D Flip-Flop circuit

- **Design Of Two Bit DAC**

Thus to digital CMOS technology, multiplexer logic has been employ to act as DAC,[18] since the purpose of DAC is to provide an analog voltage corresponding to digital bits, That means a effortless analog multiplexer can do this trade The logic equation recitation the procedure of the Multiplexer that we are using here as a 2-DAC. show in fig.7

$$Z = A(S1.S2)+B(S1.\overline{S2})+C(\overline{S1}.S2)+D(\overline{S1}.\overline{S2})$$

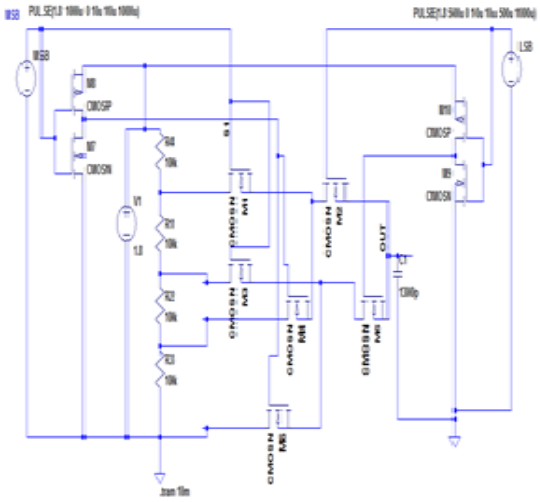

Fig.7 Design of Two Bit DAC

IV SIMULATION AND RESULT

The design and implementation of 12-bit pipeline ADC has been carried out in tsmc018 (Taiwan semiconductor manufacturing corporation) technology, but the design of pipeline ADC gets limited to 12-bit. This is a 0.18 µm in LT spice switcher CAD-III tool. The supply voltage is bipolar +/- 5(1.8v) the tool used for the design are LT spice switcher CAD-III for schematic, LT -spice for Simulation.

- **Results Of Comparator**

The dc analysis result of comparator, whose reference is set at 0.9 volt. Curve shows output of the second stage .the Transient results of the comparator show in fig.8 and fig.9.

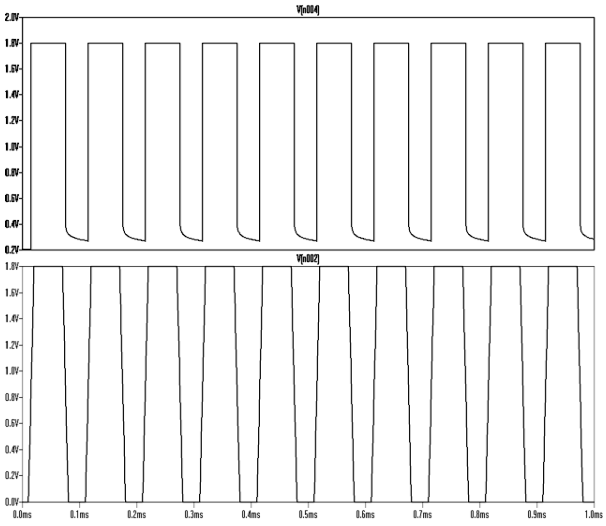

Fig 8 Transient Analysis of Comparator

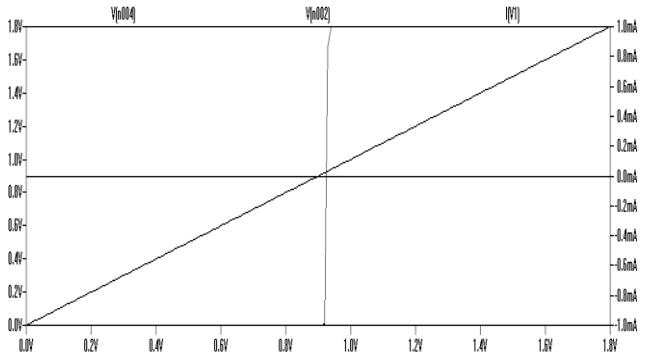

Figure 9 DC-Sweep Characteristic of Comparator

- **Results Of Sample & Hold**

The transient response of the sample &hold circuit shows in Figure 10

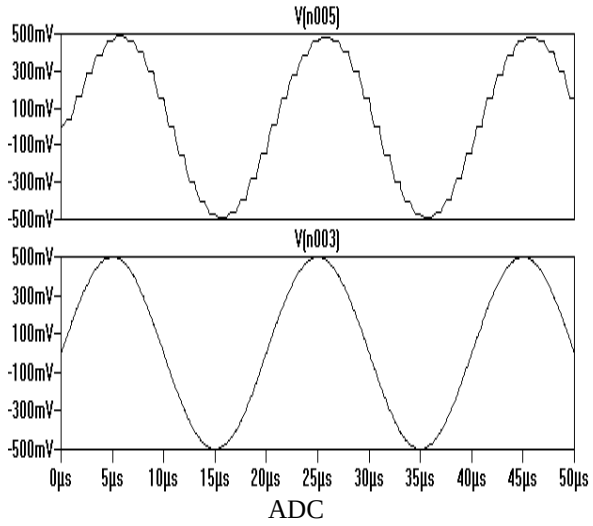

Figure 10 Transient Result of Sample & Hold Circuit

- **Results Of DAC**

The transient response of the sample &hold circuit shows in Figure 11

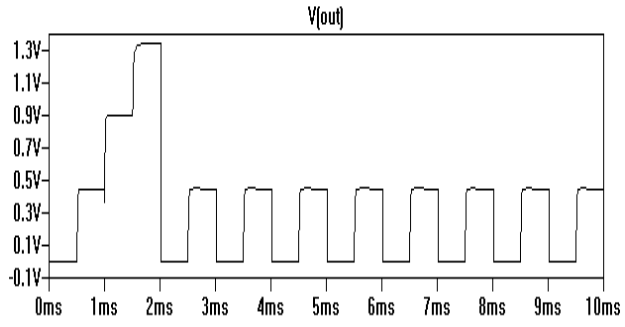

Figure 11 Transient Results of DAC

Results Of D-Flip Flop

The transient response of the sample &hold circuit shows in Figure 12

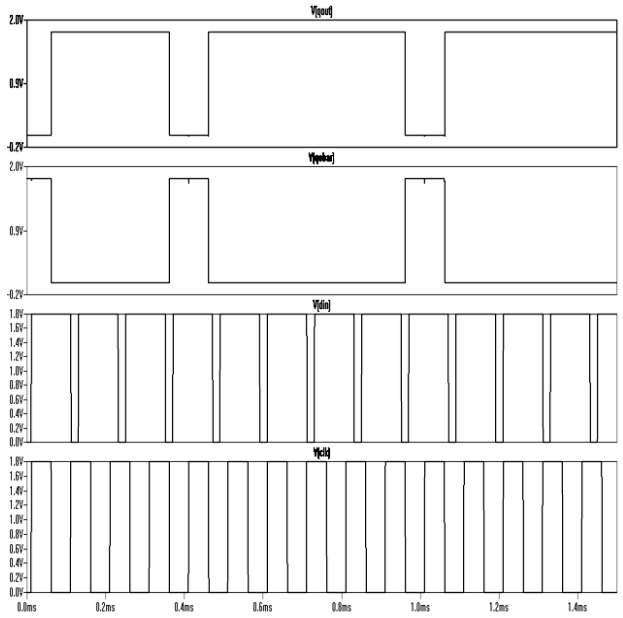

Figure 12 Transient Results of D FF

- **12 Bit Pipeline ADC Result**

Here we will describe how the pipelining is implemented by adding the sub -circuits those we have designed above**.** In first step to design pipeline we need to design Sample & hold circuit ,2-bit ADC,2-bit DAC,and a inverting Gain amplifier. Which we have designed, here we will use four stages to get the resolution of 12-bit.

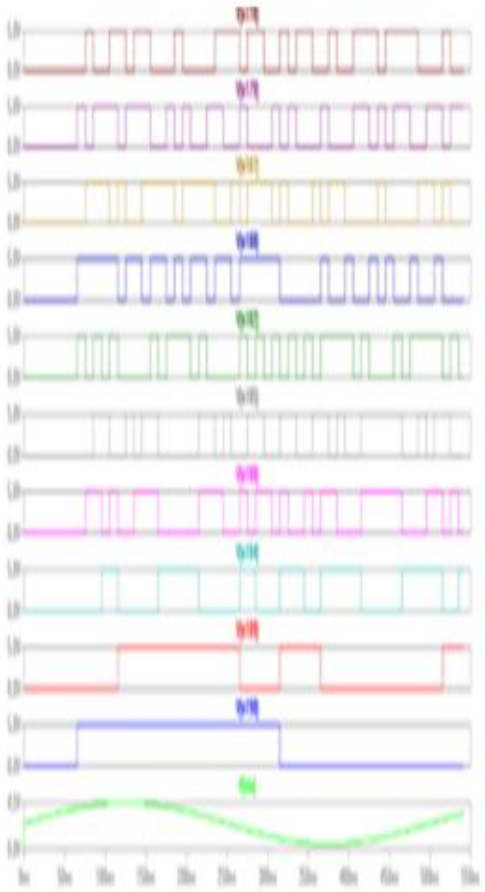

Figure 13 Transient Results of 12 bit pipeline ADC

When we apply the input signal to Sample & hold circuit. Get the sampled output and these applied to comparators and get the digital output these digital signal applied to DAC unit to analog signal and output of DAC subtracted to sampled output and amplified by inverting gain amplifier, further applied to second stage. And repeat this steps fig 13 show the six stage implementation

V Comparison

This section show comparison of implementation in term of various parameter shows in below table 1

Table 1 comparison table

Parameter	Design 1	PROPOSED
Sampling frequency	2Ghz	2GHz
Comparator	14	3 per stage
Bit per stage	1.5	2
Power dissipation	22.06Mw	437.255nW
Full scale input signal	646MHz	10.333MHz
Resolution	8 bit	12 bit

VI CONCLUSION

- The Design of 12-bit pipeline ADC has been carried out in TSMC 018µm technology. The design is implemented in LT Spice Switcher CAD –III Schematic Editor and the results are verified with LT spice and simulation viewed in LT SPICE. The key Design module is summarized now. Each block of project is designed at transistor level and design is simulated on LT spice switcher CAD –III schematic editor's simulation tool, schematic editor is used for design entry. The simulator after simulation provides respective waveforms. The design is implemented on TSMC0.18technology with feature size of 0.18 micron. The overall Design is tested with various input signals and the results are obtained
- Satisfactory for the specification implimentated of six stage we get total Resolution of 12-bit, and Supply Voltage Range = -1.8 V to + 1.8 Analog. Input Voltage Range = ± 5V. Maximum Input frequency >50MHz ,Maximum Sampling rate 20 GHz .and Unity gain inverting Amplifier is to be designed to prove buffering in Sample and Hold stage. DC Gain is 1 V/V. total Power Dissipation is 437.255nW Technology of design TSMC 0.18 µm CMOS. full scale input signal is 10.333MHz.

Because of convergence problem occurring in the tool only 12-bit design of ADC is carried out. The 12-bit pipeline ADC is working up to 1 GHZ input frequencies. The aim of the project is to design a 12-bit pipeline ADC Design parameters include input range, conversion speed, resolution, power consumption, physical dimensions, etc. This design is not targeted to one special application, so the design specifications for various application standard.

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