An Extensive Review on VLSI Computational Architecture for ACT

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Abstract- Digital signal processing (DSP) algorithms exhibit an increasing need for the efficient implementation of complex arithmetic operations. The computation of trigonometric functions, coordinate transformations or rotations of complex valued phasors is almost naturally involved with modern DSP algorithms. Discrete cosine transform (DCT) is widely used transform in image processing, especially for compression. Some of the applications of two-dimensional DCT involve still image compression and compression of individual video frames, while multidimensional DCT is mostly used for compression of video streams and volume spaces. Transform is also useful for transferring multidimensional data to DCT frequency domain, where different operations, like spread-spectrum data watermarking, can be performed in easier and more efficient manner. The ACT can also be computed non-exactly for any input sequence, with low area complexity and low power consumption, utilizing the novel architecture described. This work provide the central mathematical properties of the ACT, necessary in designing efficient and accurate implementations of the new transform method.

Keywords- DSP,ACT,DCT,VLSI,FPGA.

I. INTRODUCTION

Computers have improved dramatically in speed, memory capacity and cost over the more than forty years where operation counting has been the mainstay of algorithm analysis. These improvements have been driven largely by advancements in integrated circuit fabrication technology. In 1965, the largest integrated circuit had 64 transistors. Today, a single chip can have well over one billion transistors. These advances have produced a dramatic increase in performance and memory capacity. Remarkably, the sequential programming model has remained dominant throughout these technological advances. While parallel processors are used for large scale numerical computation, databases and, more recently, web servers, most computers have been based on a single processor CPU. With the dominance of the sequential programming model, operation counting has remained prevalent in algorithm analysis.

Digital signal processing (DSP) algorithms exhibit an increasing need for the efficient implementation of complex arithmetic operations. The computation of trigonometric functions, coordinate transformations or rotations of complex valued phasors is almost naturally involved with modern DSP algorithms.

The Fourier series representation of a continuous-time periodic signal can contain a countably finite number of frequency components because the frequency range of continuous-time signals can extend between $-\infty$ to ∞. The frequency spacing between two adjacent components is 1/Tp. Discrete-time signals have also infinite frequency range, but it is periodic, so one period is sufficient for the complete reconstruction of discrete signal. Thus, we can say that frequency range is in the interval $(-\pi,\pi)$ or $(0, 2\pi)$. If discrete signal is periodic with the fundamental period N, then its adjacent frequency components are separated by $2\pi/N$ radians.

Discrete cosine transform (DCT) is widely used in image processing, especially for compression. Some of the applications of two-dimensional DCT involve still image compression and compression of individual video frames, while multidimensional DCT is mostly used for compression of video streams. DCT is also useful for transferring multidimensional data to frequency domain, where different operations, like spread-spectrum, data compression, data watermarking, can be performed in easier and more efficient manner. A number of research works discussing DCT algorithms is available in the literature that signifies its importance and application.

The term “transform” means to change form or appearance. In terms of signal processing, a transform is normally a tool that is used to convert the signals from time domain or spatial domain to the frequency domain. There are various instances when it is pertinent to have the signal in the time domain and on the other instances it is important to have the signal in the frequency domain. For most of the image processing purposes it is better to have the signal in the frequency domain. In others words, a transformation can be described as the process of mapping the correlated data to no-correlated data. Each pixel in an image is correlated with its neighbor pixels. The information represented by any pixel should be predicted by its neighbors because of the fact that they are all correlated. DCT has been a very popular transform for many years. The fact that DCT is a near optimal transform is the main reason for its popularity.

II. DCT CALCULATION METHODS

The Discrete Cosine Transform plays a central role in most video and image compression applications the complexity of implementing an N x N 2-D DCT or IDCT directly is too great for a practical VLSI circuit. To reduce the area of these transforms, a less complex algorithm must be used. Because of the growing importance of image and video compression, a great deal of research has been done in this area and a number of algorithms have been discovered.

1. Row-Column Decomposition

One of the properties of the 2-D DCT and IDCT is that they are separable transforms. This means that the 2-D DCT can be implemented using the 1-D DCT and the 2-D IDCT can be implemented using the 1-D IDCT. Because of separability, any algorithm which reduces the complexity of the 1-D DCT will also reduce the complexity of the 2-D DCT. In order to understand separability, it is necessary to first define the 1-D DCT and IDCT. A 1-D DCT is given by equation (1).

$$y(k) = \sqrt{\frac{2}{N}}\alpha(k)\sum_{n=0}^{N-1} x(n)\cos\left[\frac{(2n+1)k\pi}{2N}\right] \ldots\ldots(1)$$

and a 1D, IDCT is given by equation 2

$$x(n) = \sqrt{\frac{2}{N}}\sum_{n=0}^{N-1} \alpha(k)\,x(n)\cos\left[\frac{(2n+1)k\pi}{2N}\right] \ldots\ldots(2)$$

Where x is an Nxl vector of input pixels and v is an Nxl vector of 1-D DCT coefficients.

Separability is a way of calculating a 2-D transform using a 1-D transform. Specifically, separability means that the 2-D transforms can be performed by doing a 1-D transform on each row of the input matrix and then doing a 1-D transform on each column of the intermediate result. This technique is often called row/column decomposition.

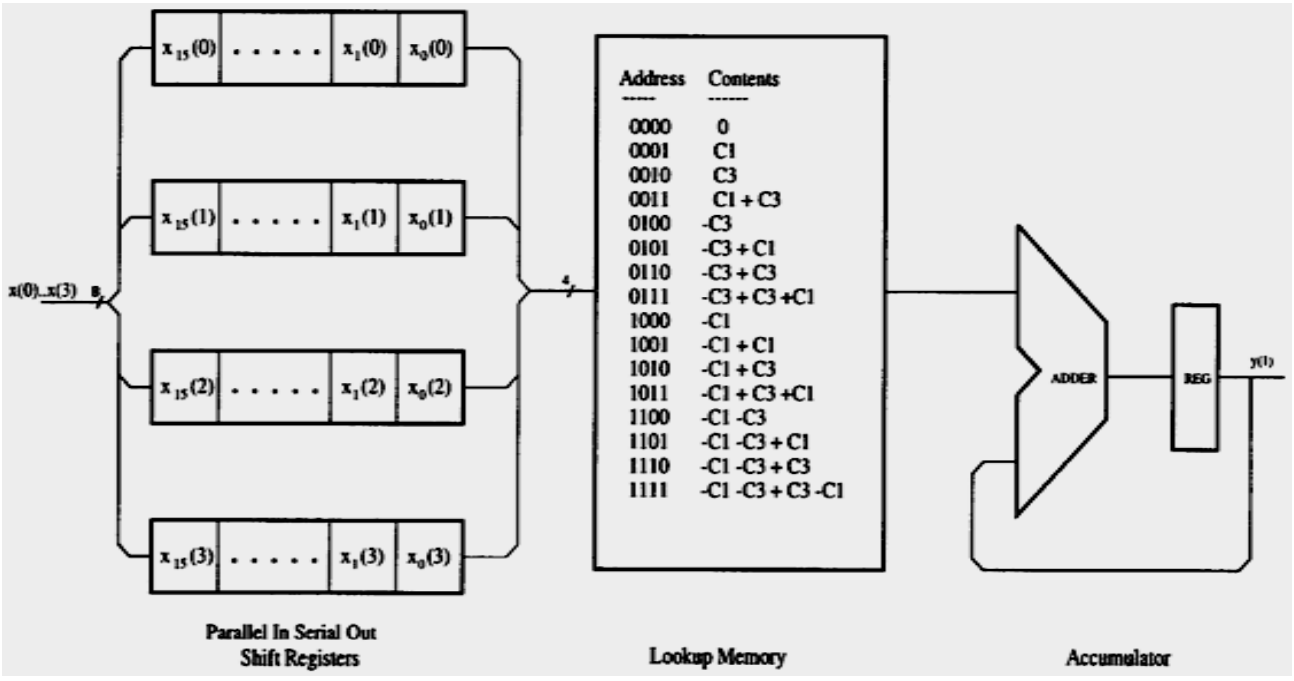

Figure 2.2 Circuits to Compute One Point of a 4-Point DCT Using DA

2. Flowgraph Algorithms

Flowgraph decomposition is the same technique which was used to derive the Fast Fourier Transform from the Discrete Fourier Transform. The basic idea is to decompose an N-point transform into 2 transforms of length y. Since an N- point DCT requires N2 multiplications and additions, two y -point DCT's require 2 (y) or fy multiplications and additions. If this technique is applied recursively, the original N-point DCT can be reduced to y 2-point DCT's. The number of multiplications and additions required to compute the transform falls from N2 to roughly $Nlog2N$.

3. Distributed Arithmetic

Distributed arithmetic (DA) was proposed by Peled and Liu as a bit-serial technique for computing the cross product of two vectors without multipliers if one of the vectors is constant. While this technique was originally proposed for use with digital filters, Sun showed that it could be applied to a 1-D DCT or IDCT. To illustrate,

consider the vector multiply used to obtain y(1), one point of a 4-point DCT:

$$y(1) = [C_1, C_3, -C_3, -C_1] \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \end{bmatrix} \dots\dots\dots\dots (3)$$

The column vector of inputs, $x(0)$ through$x(3)$, can be rewritten as a matrix of bits in which the nth row is a vector of l's and 0's expressing $x(n)$ as a two's complement.

Figure 2.2 shows a block diagram of a circuit which calculates y(l) using this technique. The circuit consists of four parallel-in serial-out (PISO) shift registers, a lookup table memory and an accumulator.

III. PREVIOUS WORK

N. Rajapaksha, A. Madanayake, R. J. Cintra, J. Adikari and V. S. Dimitrov,[1] The discrete cosine transform (DCT) is a widely-used and important signal processing tool employed in a plethora of applications. Typical fast algorithms for nearly-exact computation of DCT require floating point arithmetic, are multiplier intensive, and accumulate round-off errors. Recently proposed fast algorithm arithmetic cosine transform (ACT) calculates the DCT exactly using only additions and integer constant multiplications, with very low area complexity, for null mean input sequences. The ACT can also be computed non-exactly for any input sequence, with low area complexity and low power consumption, utilizing the novel architecture described. However, as a trade-off, the ACT algorithm requires 10 non-uniformly sampled data points to calculate the eight-point DCT. This requirement can easily be satisfied for applications dealing with spatial signals such as image sensors and biomedical sensor arrays, by placing sensor elements in a non-uniform grid. In this work, hardware architecture for the computation of the null mean ACT is proposed, followed by a novel architecture that extend the ACT for non-null mean signals. All circuits are physically implemented and tested using the Xilinx XC6VLX240T FPGA device and synthesized for 45 nm TSMC standard-cell library for performance assessment.

T. S. Elias and P. B. Dhanusha,[2] The research work describes the design of one-dimensional discrete cosine transform (DCT) which is widely used in image and video compression systems. The objective of this research work is to design an area efficient fully parallel distributed arithmetic (DA) architecture for one-dimensional DCT to be implemented on field programmable gate array (FPGA). DCT requires large amount of mathematical computations including multiplications and accumulations. The multipliers consume increased power and area; hence multipliers are completely discarded in the proposed design. Distributed arithmetic is a method of modification at bit stream for sum of product or vector dot product to hide the multiplications. DA is very much suitable for FPGA designs as it reduces the size of a multiply and accumulate hardware. The speed is increased in the proposed design with the fully parallel approach. In this work, existing DA architecture for 1D-DCT and the proposed area efficient fully parallel DA architecture for 1D-DCT are realized. The simulation is performed using Modelsim6.2b and synthesized with Xilinx IS E Simulator. The 1D-DCT can be extended to 2D-DCT by using row column decomposition technique.

M. W. Lee, J. H. Yoon and J. Park,[3] This research work presents a low-power coordinate rotation digital computer (CORDIC)-based reconfigurable discrete cosine transform (DCT) architecture. The main idea of this research work is based on the interesting fact that all the computations in DCT are not equally important in generating the frequency domain outputs. Considering the importance difference in the DCT coefficients, the number of CORDIC iterations can be dynamically changed to efficiently tradeoff image quality for power consumption. Thus, the computational energy can be significantly reduced without seriously compromising the image quality. The proposed CORDIC-based 2-D DCT architecture is implemented using 0.13 μm CMOS process, and the experimental results show that our reconfigurable DCT achieves power savings ranging from 22.9% to 52.2% over the CORDIC-based Loeffler DCT at the cost of minor image quality degradations.

M. Jridi, P. K. Meher and A. Alfalou,[4] One promising solution to reduce the computational complexity of discrete cosine transform (DCT) is to identify the redundant computations and to get rid of them. In this study, the authors present a new method to predict zero-quantised DCT coefficients for efficient implementation of intra-frame video encoding by identifying such redundant computations. Traditional methods use the Gaussian statistical model of residual pixels to predict all-zero or partial-zero blocks. The proposed method is based on two key ideas. At first, the bounds of DCT coefficients are derived from the intermediate signals of the Loeffler DCT algorithm instead of calculating the sum of absolute difference (SAD) of residual pixels. The sufficiency conditions are then suitably chosen to predict the zero-quantised coefficients to reduce the arithmetic complexity without degrading the video quality. Simulation results are found to validate the analytical model and show that the proposed prediction eliminates more redundant computations than the existing methods. Moreover, the authors have derived a pipelined VLSI architecture of the

proposed prediction scheme which offers a saving of more than 63 and 91% of multiplications of the second stage of one-dimensional DCT for high and low bit-rate intra-video encoding, respectively.

H. Huang and L. Xiao,[5] This letter proposes a novel coordinate rotation digital computer (CORDIC)-based fast radix-2 algorithm for computation of discrete cosine transformation (DCT). The proposed algorithm has some distinguish advantages, such as Cooley-Tukey fast Fourier transformation (FFT)-like regular data flow, uniform post-scaling factor, in-place computation and arithmetic-sequence rotation angles. Compared to existing DCT algorithms, this proposed algorithm has lower computational complexity. Furthermore, the proposed algorithm is highly scalable, modular, regular, and suitable for pipelined VLSI implementation. In addition, this letter also provides an easy way to implement the reconfigurable or unified architecture for DCTs and inverse DCTs.

V. K. Sharma, K. K. Mahapatra and U. C. Pati, [6] Discrete cosine transform (DCT) is widely used in image and video compression standards. This research work presents distributed arithmetic (DA) based VLSI architecture of DCT for low hardware circuit cost as well as low power consumption. Low hardware cost is achieved by exploiting redundant computational units in recent literature. A technique to reduce error introduced by sign extension is also presented. The proposed 1-D DCT architecture is implemented in both the Xilinx FPGA and Synopsys DC using TSMC CLN65GPLUS 65nm technology library. For power and hardware cost comparisons, recent DA based DCT architecture is also implemented. The comparison results indicate the considerable power as well as hardware savings in presented architecture. 2-D DCT is implemented using row column decomposition by the proposed 1-D DCT architecture.

IV. PROBLEM STATEMENT

The ACT algorithm is suitable for calculating the eight-point DCT coefficients exactly using only adders and integer constant multiplications, also with low computational complexity. Hardware implementations are especially interesting for the realization of highly parallel algorithms that can achieve much higher throughput than software solutions. In addition, special purpose DCT hardware discharges the computational load from the processor and therefore improves the performance of complete multimedia system. The throughput is directly influencing the quality of experience of multimedia content. Another important factor that influences the quality of is the finite register length effect on the accuracy of the forward-inverse transformation process. The Discrete Cosine Transform is one of the most widely transform techniques in digital signal processing. Hence the motivation for the design of the high performance with reduced complexity Discrete Cosine transform architecture is clear.

V. CONCLUSION

In the work present and study various DCT and IDCT algorithms and their performance and hardware implementation. The Discrete Cosine Transform is one of the most widely transform techniques in digital signal processing. This is also most computationally intensive transforms which require many multiplications and additions. Real time data processing necessitates the use of special purpose hardware which involves hardware efficiency as well as high throughput. Many DCT algorithms reviewed in order to achieve high speed DCT. Those architectures which involves multipliers for example Chen's algorithm has less regular architecture due to complex routing and requires large silicon area. Popular application examples are algorithms used in digital communication technology and in adaptive signal processing. There are several issues are observed regarding the implementation of DCT. The main issue of its kind is timing issues. The area and issues are not optimized for any of the three designs.

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