A Survey On 12 Bit Pipe Line Analog To Digital Converter Using CMOS Technology

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Abstract - This Paper presents a novel technique for design of 12 bit resolution pipe line analog to digital converter. A special comparator with built-in threshold inverter quantization is also discussed for the implementation of pipeline ADC which is reduce area of pipe line ADC and reduced the power consumption. This Design is implemented and verified on the LT spice switcher CAD-III in 0.18µm Technology. The circuit, designed and simulated in a 0.18µm CMOS technology, The supply voltage is -5v to +5v the simulated power consumption is less than50 mw, Analog Input Voltage Range = ± 5V Maximum Sampling rate >40 MHz Sample and Hold stage. DC Gain= 1 V/V Power Dissipation = ≥ 25mw ,Maximum input frequency >50MHz,Maximum Sampling rate > 40 MHz, Sample and Hold stage. DC Gain= 1 V/V.

Key words : Pipe Line ADC ,S/H circuit, DAC, TIQ comparator.

INTRODUCTION

THE pipelined ADC architecture has been adopted into many high-speed applications including high-performance digital communication systems and high-quality videos systems [1], [2]. The rapid growth in these application areas is driving the design of ADCs toward higher operating speed, lower power consumption and smaller die size. The continuing trend of submicron CMOS technology scaling, which is coupled with lower power supply voltages, makes it possible to keep up with the application development. However, this trend poses challenges to conventional pipelined ADC designs. As a result, the finite op-amp gain is becoming a major hurdle in achieving both high speed and high accuracy.

The proposed ADC utilizes the Threshold Inverter Quantization (TIQ) technique that uses two cascaded CMOS inverters as a comparator. The TIQ technique has been introduced in [3]. The TIQ technique proposed here has been developed for better implementation in SOC applications.

II PIPELINED ADC

A pipelined analog-to-digital converter (ADC) architecture which is suitable for low power and small area is presented. The pipelined ADC architecture is a type of sub-ranging ADC introduced in the previous section. This architecture is implemented with at least two or more low resolution flash ADCs as shown in Figure 2.8. Each stage has a S/H circuit to hold the amplified residue from the previous stage. Then, the input is fed to the low resolution flash ADC to generate a segmented binary output. Like the sub-ranging ADC, the segmented output is changed to an analog signal and is subtracted from the input. This residue is amplified in an amplifier to send to the next stage. The segmented binary outputs from each stage are time-aligned with a shift register. The final binary output is obtained after passing through digital error correction logic. This conversion process in the pipelined ADC is shown in Figure 1.

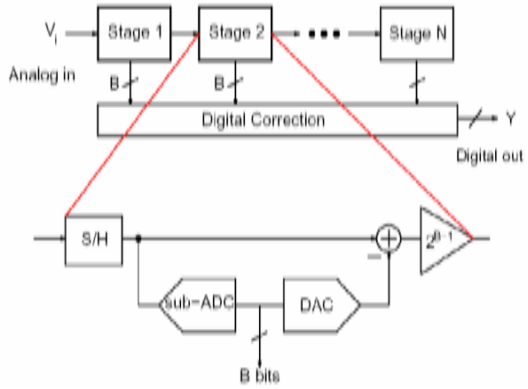

Figure 1 block diagram of pipelined ADC

As shown in Figure 1, the internal flash ADCs have low resolution that depends on the application. Hence, the pipelined ADC can be applied from high speed applications with low resolution to low speed applications with high resolution. Also it can be modified for low power applications. They provide effective signal bandwidths equal of 10-100 MHz (sample rates of 20-200 MHz). The conversion mechanism is similar to that of sub-ranging conversion In each stage.

II PROPOSED DESIGN

Pipeline architectures transfer the residual from one stage to another. An amplification factor relaxes the accuracy requirements of the successive stage. The limit to accuracy for conventional pipelines comes from the ADC, the DAC and the analog blocks used to generate the residual

The aim of the project is to design a 12-bit pipeline ADC Design parameters include input range, conversion speed, resolution, power consumption, physical dimensions, etc. This design is not targeted to one special application, so the design specifications are not strictly following any

application standard. The general guideline is to design a high speed, low power pipeline ADC with wide input bandwidth. Each block of project is designed at transistor level and design is simulated on LT Spice Switcher CAD –III schematic editors simulation tool, schematic editor (is used for design entry. The simulator after simulation provides respective waveforms. The design is implemented on TSMC018 technology with feature size of 0.18 micron.

III DESIGN SPECIFICATIONS

- Resolution = 12-bit
- Supply Voltage Range = -1.8 V to + 1.8 V
- Analog Input Voltage Range = ± 5V
- Maximum Input frequency >50MHz
- Maximum Sampling rate >40 MHz
- Sample and Hold stage. DC Gain= 1 V/V
- Power Dissipation = ≥ 25mw
- Technology of design : TSMC 0.18 µm CMOS

III SINGLE STAGES ADC DESIGN

As the through put should be as fast as of flash ADC, so each stage of the pipeline ADC is inherited form flash architecture. The resolution of each stage will decide how many comparators are required, what will be the latency of the system, what kind of DAC architecture has to be incorporated, need of fast encoding circuitry. For example, if we choose 3 bits per stage, than for 7 bit pipeline ADC, there will be total three stages one will comprises of one bit ADC and remaining will have 3 bit ADC architecture, thus the total number of comparator required are $35(2^3+2^3+1-2)$ also it will require two (2 bit) and one (1 bit) DAC. Since the selected architecture comprises of one bit ADC this only one comparator is required and total number of comparator will be 7, drastically reduced This is the reason, which will simplify the design of other sub-blocks of each stage, for example design of DAC and associated digital circuitry. Figure 2 shows are architecture of each stage of pipeline ADC.ADC For the design of each stage of pipeline ADC (shown in figure 3), the required components are

- Sample and Hold,
- Amplifier configure for gain of 4.
- Analog Adder,
- 2-bit DAC
- 3-Comparator.

IV LITERATURES

J. Aria set al Methodology Pipe Line ADC& timing interleaving Better performance The ADC exhibits a good performance for the demodulation of OFDM Better resolution for low frequency signals this paper was 10 bit analog to digital converter with 12 Mw power dissipation in this paper pipe line and time interleaving both architecture have been used this circuit fabricated with 0.25µm CMOS technology with 12mW power supply It is a nine-stage 1.5-bit/stage time-interleaved dual-pipeline converter[8]. One pipeline processes the even samples, while the other pipeline works on odd samples. Both pipelines share their operational amplifiers (OPAMPS) [9]. This constitutes a large power saving, because OPAMPS are the most power-demanding blocks, and helps to minimize offset and gain mismatches between pipelines that could degrade the ADC's performance

Zhuang Zhaodongetal. In this design, 7 bit resolution was implemented by pipelined analog to digital converter. The power dissipation for this circuit was very low, at about 3.7mw due to the ideal components used for designing the circuit. The design was fabricated using 0.18 µ m CMOS technology and the design is implemented in TSMC 018 CMOS technology. Internal flash ADC is 3-bit per stage used which increases the comparator size, thereby increasing the circuit complexity because flash ADC consists of an 2^{n-1} to comparators. Since resolution increases with the comparators size, this pipelined ADC architectures were studied in proposed work. In this work, a 2-bit internal flash is used and resolution & gain have been enhanced.

S.W. Ross, Student et.al Allow a large range of functionality use in communication A 75 MS/s Pipeline ADC is used as an example here to elaborate the system level design. This section describes how determination of system level parameter is chosen from a given set of pipeline ADC specifications.

Andreas Santneret.al Flash Pipelined ADC ADCs are suitable for a broadband mobile communication terminal. and for wireless receivers The maximum input frequency being 1GHz, we select a sampling frequency of 2.2GHz. We also want a minimum Signal-to-Noise Ratio (SNR) of 50dB. This value leads to 10 bits of resolution. Of course, low consumption and highly relevant objectives in such mass devices. ADCs are often characterized by the sampling rate and the resolution. This latter is defined by the SNR and the Effective Number of Bits (ENOB). Surface and power consumption are key elements when addressing a market

V SCOPE OF RESEARCH

There are various parameter on which research can be find out such as bandwidth ,sampling rates ,resolution

- Increase resolution
- Increase multi bit per stage

- Reduce power dissipation
- Reduce chip area

V CONCLUSION

The Design of 12-bit pipeline ADC is to be design in TSMC0.18µm technology. The design is implemented in LT Spice Schematic Editor and the results are verified with CAD-III. The key Design module is summarized now.3-TIQ Comparator will be used in single stage of ADC. An Analog multiplexer will be used as DAC. An .total power dissipation less than 24 mw ,resolution 12bit.

VI REFERENCES

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