# A Review on Fast and Low power Binary to BCD Conversion for B/D Multi-Operand Adder

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***Abstract - Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Binary to BCD conversion forms the basic building block of decimal digit multipliers. This paper presents novel high speed low power architecture for binary to BCD conversion which is at least 50% better in terms of power-delay product and 80% in area than the existing designs. Decimal data processing applications have grown exponentially in recent years and the IEEE 754-2008 standard for floating point arithmetic has already dictated the importance of decimal arithmetic. The design will be implemented on Xilinx and simulation will be carried out by the I-Sim simulator.***

***Key words: Binary To BCD Conversion, Ripple Adder, Add-3 Algorithm.***

## 1 INTRODUCTION

The binary numbering system is, by far, the most common numbering system in use in computer systems today. In days long, however, there were computer systems that were based on the decimal (Base 10) numbering system rather than the binary numbering system. Such computer systems were very popular in systems Targeted for business/commercial systems. Although systems Designers have discovered that binary arithmetic is almost always better than decimal arithmetic for General calculations, the myth still persists that decimal arithmetic is better for money calculations than binary arithmetic. Therefore, many software systems still specify the use of decimal arithmetic in their calculations [16]. This paper introduces a multi-operand decimal addition algorithm by employing high speed binary to BCD converter circuit, which speeds up the process of decimal addition when multiple BCD operands are added together. A Novel design for 16-bit binary to BCD converter circuit is proposed. Further, analysis is done with respect to the existing binary to BCD converter architectures. The proposed algorithm is fundamentally different from multi-operand BCD addition algorithms [3, 5] since intermediate BCD corrections are not done rather correction is done at the final stage to get proper BCD results.

## 2 BCD CONVERTERS

Binary Coded Decimal is that number system or code which has the binary numbers or digits to represent a decimal number. A decimal number contains 10 digits (0-9). Now the equivalent binary numbers can be found out of these 10 decimal numbers. In case of BCD the binary number formed by four binary digits, Will be the equivalent code for the given decimal digits. In BCD we can use the binary number from

0000-1001 only, which are the decimal equivalent from 0-9 respectively. In the proposed binary to decimal converter for conversion process we use shift and add 3 algorithms.

## 3 PROPOSED ALGORITHM

Though the shifting and adding by 3 algorithms is not novel, the architecture execution by means of adding by constant which ultimately makes it area efficient is The most important objective of proposed algorithm is to perform proficient fixed bit binary coded decimal conversion. [24]

## 4 DESCRIPTION OF THE ALGORITHM

The fundamental idea is to shift the binary number left, one bit in one time, into position revert for the BCD results. Let us receive the mode of the binary number 8'h7C. This is to be modifying into a 12-bit/3 digital BCD result as shown below. After 8 shift operations, the three BCD digits enclose individual: hundredth digit = 4'b0001, tens digit = 4'b0010 and ones digit = 4'b0100, thus representing the BCD assessment of 124.

The idea following the algorithm can be stated as follows:-

1. Each time the number is shifted left; it is multiplied by 2 as it is change to the BCD position;
2. The value inside the BCD digits is the similar as binary till 9 binary numbers or less than 9 binary numbers. Though if it is 10 or higher than it is not correct BCD number because for BCD, this should carry over after that digit. An improvement has to be needed and this can be made through adding 6 to this binary digit.
3. The simplest approach to do this is to distinguish if the value inside the BCD digit locations are 4 or above previous to the shift (i.e. X2). If it is ≥5, then

4. The hardware to achieve binary toward BCD add 3 to the value (i.e. adjust by +6 after the shift). [1]

Conversion is shown below. Shifting is simple – just wire all signals one location to the left. For every one of the BCD locations, we need an "adjust" module which execute and go behind operation: if the value is ≥5, then add 3. This is best illustrated using our example;-

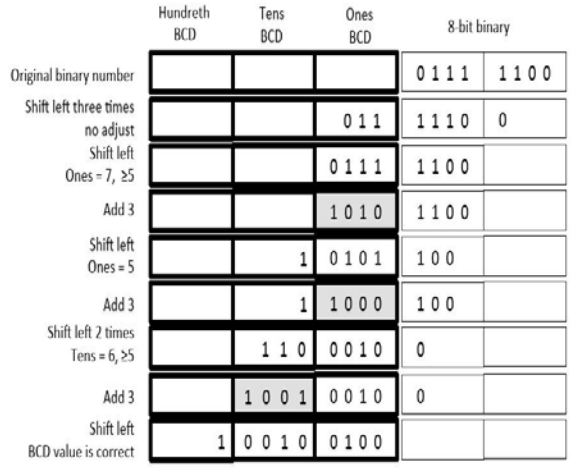


Fig. 1 shown add-3 algorithm

- Binary number left one bit. If 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column.
- If the binary value in any of the BCD columns is 5 or greater, add 3 to that value in that BCD column. Repeat the above process.

## 5 LITERATURE SURVEY

Several algorithms had been already proposed by [6], [8-10] for binary to decimal conversion, which improve speed, delay, power consumption and area of chip. [6] Has proposed and implemented a new, fresh and highly efficient hardware algorithms, but it gives wrong outputs to some decimal values as shown in table III. [8] Has also proposed an optimized version of [6]'s architecture by using logical equations and optimized DL block, but it is also giving wrong outputs of the following values (50, 56) as shown in table III. These errors are occurring because the proposed algorithm isn't correct for some special cases and there are some architecture level faults too. In the next section we are giving explanation of the above errors and give proper improvement in proposed algorithm and architecture of [6, 8].

**Alp Arslan Bayrakci et al.** proposed a BCD adder with efficient carry generation using analyzer circuit. The circuit performs well in terms of delay compared to architectures mentioned in literature and shows better area performance. Anshwal Singh et al.,[9] designed a novel architecture for BCD addition and subtraction . The design uses three major blocks viz., PG block, prefix block and the correction block and generates carry without any extra logic thus performing better in terms of area performance compared to the BCD adder in [10]. **Sundaresan.C et al.**

in a pioneer work on design of Reduced delay BCD adder used Carry Look Ahead (CLA) adder in the initial stage being followed by carry network and correction logic in the second and third stages. Though the circuit is fast compared to the architecture in [12], the use of CLA adder in initial stage increases area cost. Chetan Kumar et al., [12] presented a unified architecture for BCD and binary addition. Though the circuit has lower delay compared to the architectures mentioned in literature the design of post correction circuitry poses problems for multi-bit operands.

**Osama Al-khaleel et al.** proposed a correction free BCD adder in which the input operands are split and added in two stages. Stage 1 adds the MSB three bits of a four bit BCD number and the result out of stage 1 is passed to stage 2 and added with the LSB. The latency of the architecture is very less compared to the architectures mentioned in literature.

**H. Neto and M. Vestia et,al.** Decimal arithmetic has become a major necessity in computer arithmetic operations associated with human-centric applications, like financial and commercial, because the results must match exactly those obtained by human calculations. In this work, a novel approach is introduced to the design of a decimal (BCD) multiplier.

**A. Guntoro and M. Glesner et.al** This paper presents the design and the implementation of an FPGA-based floating-point adder with three inputs. It can be used in Discrete Wavelet Transform (DWT) applications. The design is based on a 5-level pipeline stage in order to distribute the critical paths and to maximize the performance. The data dependencies to minimize the number of the pipeline stages and to reduce the resource allocation are examined

## 7 CONCLUSIONS

In this proposed approach, which consist of a ripple save adder and binary to BCD converter gets a better result compared to the existing design and simulation results shows the delay and area variations which is a key advantage

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