Design of Low Complexity Concurrent Fault Deduction and Correction for Parallel FFTs

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Abstract - As signal-processing circuits become more complex, it is common to find several filters or FFTs operating in parallel. Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic- based fault tolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT. One example is fast Fourier transforms (FFTs) that are a key building block in many systems. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, probably the use of the Parseval or sum of squares checks is the most widely known. In modern communication systems, it is increasingly common to find several blocks operating in parallel. Recently, a technique that exploits this fact to implement fault tolerance on parallel filters has been proposed. In this brief, this technique is first applied to protect FFTs. Then, two improved protection schemes that combine the use of error correction codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection.

Keywords—FFTs, ABFT, Parseval check.

1. INTRODUCTION

The complexity of communications and signal processing circuits increases every year. This is made possible by the CMOS technology scaling that enables the integration of more and more transistors on a single device. This increased complexity makes the circuits more vulnerable to errors. At the same time, the scaling means that transistors operate with lower voltages and are more susceptible to errors caused by noise and manufacturing variations .The importance of radiation-induced soft errors also increases as technology scales .Soft errors can change the logical value of a circuit node creating a temporary error that can affect the system operation. To ensure that soft errors do not affect the operation of a given circuit, a wide variety of techniques can be used. These include the use of special manufacturing processes for the integrated circuits like, for example, the silicon on insulator. Another option is to design basic circuit blocks or complete design libraries to minimize the p one classical example is the use of triple modular redundancy (TMR) that triples a block and votes among the three outputs to detect and correct errors. The main issue with those soft errors mitigation techniques is that they require a large overhead in terms of circuit implementation. For example, for TMR, the overhead is >200%. This is because the

unprotected module is replicated three times (which requires a 200% overhead versus the unprotected module), and additionally, voters are needed to correct the errors making the overhead >200%.

This overhead is excessive for many applications. Another approach is to try to use the algorithmic properties of the circuit to detect/correct errors. This is commonly referred to as algorithm- based fault tolerance (ABFT). This strategy can reduce the overhead required to protect a circuit. Signal processing and communications circuits are well suited for ABFT as they have regular structures and many algorithmic properties. Over the years, many ABFT techniques have been proposed to protect the basic blocks that are commonly used in those circuits. Several works have considered the protection of digital filters. For example, the use of replication using reduced precision copies of the filter has been proposed as an alternative to TMR but with a lower cost. The knowledge of the distribution of the filter output has also been recently exploited to detect and correct errors with lower overheads. The protection of fast Fourier transforms (FFTs) has also been widely studied. As signal-processing circuits become more complex, it is common to find several filters or FFTs operating in parallel. This occurs for example in filter banks or in multiple-input multiple-output (MIMO) communication systems. In particular, MIMO orthogonal frequency division modulation (MIMO-OFDM) systems use parallel iFFTs/FFTs for modulation/demodulation. MIMO- OFDM is implemented on long-term evolution mobile systems and also on WiMax. The presence of parallel filters or FFTs creates an opportunity to implement ABFT techniques for

the entire group of parallel modules instead of for each one independently.

This has been studied for digital filters initially where two filters were considered. More recently, a general scheme based on the use of error correction codes (ECCs) has been proposed. In this technique, the idea is that each filter can be the equivalent of a bit in an ECC and parity check bits can be computed using addition. This technique can be used for operations, in which the output of the sum of several inputs is the sum of the individual outputs. This is true for any linear operation as, for example, the discrete Fourier transform (DFT). Rob ability of soft errors. Finally, it is also possible to add redundancy at the system level to detect and correct errors.

2. PROPOSED METHOD

Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic-based fault tolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT. One example is fast Fourier transforms (FFTs) that are a key building block in many systems. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, probably the use of the Parseval or sum of squares checks is the most widely known.

In modern communication systems, it is increasingly common to find several blocks operating in parallel. Recently, a technique that exploits this fact to implement fault tolerance on parallel .filters has been proposed. In this brief, this technique is first applied to protect FFTs. Then, two improved protection schemes that combine the use of error correction codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection.

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2.1 PARALLEL CORRECTION METHOD:

This method is used to find, detect and correct multiple errors. It has been mentioned that over the years, many techniques have been proposed to protect the FFT. One of them is the

Sum of Squares (SOSs) check that can be used to detect errors. The SOS check is based on the Parseval theorem that states that the SOSs of the inputs to the FFT are equal to the SOSs of the outputs of the FFT except for a scaling factor. This relationship can be used to detect errors with low overhead as one multiplication is needed for each input or output sample (two multiplications and adders for SOS per sample).

For parallel FFTs, the SOS check can be combined with the ECC approach to reduce the protection overhead. Since the SOS check can only detect errors, the ECC part should be able to implement the correction. This can be done using the equivalent of a simple parity bit for all the FFTs. In addition, the SOS check is used on each FFT to detect errors.

When an error is detected, the output of the parity FFT can be used to correct the error. This is better explained with an example. In the first proposed scheme is illustrated for the case of four parallel FFTs. A redundant (the parity) FFT is added that has the sum of the inputs to the original FFTs as input. An SOS check is also added to each original FFT. In case an error is detected (using *P*1, *P*2, *P*3, *P*4*)*, the correction can be done by recomputing the FFT in error using the output of the parity FFT (*X*) and the rest of the FFT outputs. For example, if an error occurs in the first FFT, *P*1 will be set and the error can be corrected by doing

$$X_1c = X - X_2 - X_3 - X_4.$$

This combination of a parity FFT and the SOS check reduces the number of additional FFTs to just one and may, therefore, reduce the protection overhead. In the following, this scheme will be referred to as parity-SOS.

The starting point for our work is the protection scheme based on the use of ECCs that was presented in for digital filters. This scheme is shown in Fig. 2.1. In this example, a simple single error correction Hamming code is used. The original system consists of four FFT modules and three redundant modules is added to detect and correct errors. The inputs to the three redundant modules are linear combinations of the inputs and they are used to check linear combinations of the outputs. For example, the input to the first redundant module is

$$x_5=x_1+x_2+x_3 \quad (1)$$

And since the DFT is a linear operation, its output *z*5 can be used to check that

$$z_5=z_1+z_2+z_3 \quad (2)$$

This will be denoted as *c*1 check. The same reasoning applies to the other two redundant modules that will provide checks *c*2 and *c*3. Based on the differences observed on each of the checks, the module on which the error has occurred can be determined. Once the module in error is known, the error can be corrected by reconstructing its output using the remaining modules. For example, for an error affecting *z*1, this can be done as follows:

$$z_1c[n] = z_5[n] - z_2[n] - z_3[n]. \quad (3)$$

Similar correction equations can be used to

correct errors on the other modules. More advanced ECCs can be used to correct errors on multiple modules if that is needed in a given application. The overhead of this technique is lower than TMR as the number of redundant FFTs is related to the logarithm of the number of original FFTs. For example, to protect four FFTs, three redundant FFTs are needed, but to protect eleven, the number of redundant FFTs in only four. This shows how the overhead decreases with the number of FFTs.

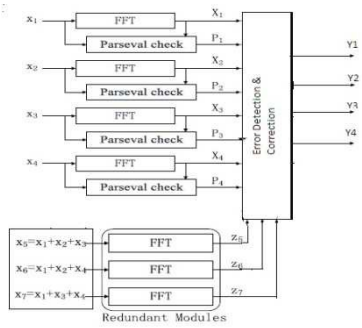
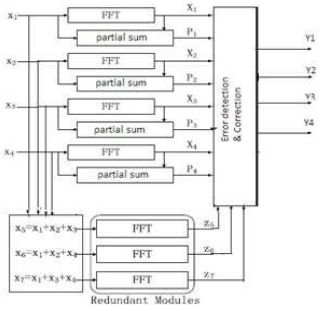


Fig 2.1 Parallel correction method

2.2 Partial summation method:

In this method sum of the input should be equal to first output, both multiple error correction and detection can be done.



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3. EXPERIMENTAL RESULTS

3.1 PROPOSED METHOD SIMULATION RESULT:

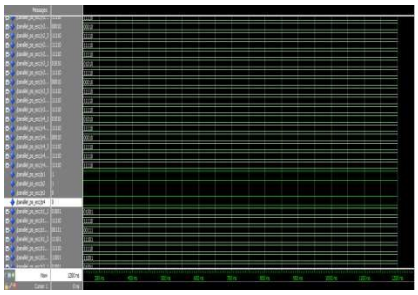

Fig 3.1 output of Parallel correction

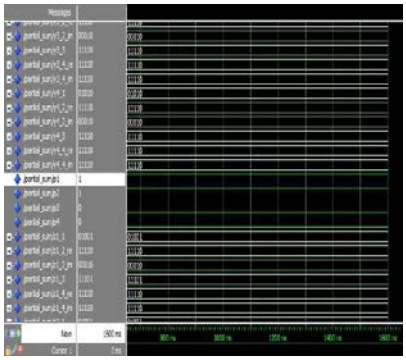

Fig 3.2 output of partial Summation

3.1.1 OUTPUT OF XILINX RESULT:

Table 3.1

Existing method	Area	Power
ECC	16735	263
Parity-SOS	10561	253
Parity-SOS-ECC	9584	252

Table 3.2

Proposed Method	Area	Power
Parallel Correction	11837	257
Partial Summation	6948	246

4. CONCLUSION AND FUTURE WORK:

In existing method it's only possible to detect the error but cannot correct the error, all detection and correction is single .As a result there will be more area and power consumption.

In proposed method multiple errors can be detected as well as corrected, hence the number fft counts are reduced. So that there will be less area and power consumption compared to existing method.

Future work Iam going to implement in the application. The application is based on Multiple input multiple output-Orthogonal frequency division multiplexing(MIMO-OFDM).

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