An Extensive Review on a Normal I/O Order Radix-2 FFT Architecture

Pratibha Gupta[1], Prof. Ashish Raghuwanshi[2]

[1]M-Tech Research Scholar, [2]Research Guide Department of Electronics & Communication Engineering, IES, Bhopal

Abstract: -The Fast Fourier Transform (FFT) is one of the most widely used digital signal processing algorithms. While advances in multiple processing technologies have enabled the performance and integration of FFT process to increase steadily, these advances have also caused the power consumption by system process to increase as well. This power increase has resulted in a situation where the number of potential FFT applications limited by maximum power budgets—not performance—is significant and growing.

Index Terms- Fast Fourier transforms (FFT), multipath delay commutator (MDC) FFT, and normal order.

I. INTRODUCTION

The Discrete Fourier Transform (DFT) is one of the most widely used digital signal process-ing (DSP) algorithms. DFTs are almost never computed directly, but instead are calculated using the Fast Fourier Transform (FFT), which comprises a collection of algorithms that efficiently calculate the DFT of a sequence. The number of applications for FFTs continues to grow and includes such diverse areas as: communications, signal processing, instrumentation, biomedical engineering, sonics and acoustics, numerical methods, and applied mechanics.

As semiconductor technologies move toward finer geometries, both the available performance and the functionality per die increase. Unfortunately, the power consumption of processors fabricated in advancing technologies also continues to grow. This power increase has resulted in the current situation, in which potential FFT applications, formerly limited by available performance, are now frequently limited by available power budgets. The recent dramatic increase in the number of portable and embedded applications has contributed significantly to this growing number of power-limited opportunities.

The Fast Fourier Transform (FFT)

The term “fast Fourier transform” was originally used to describe the fast DFT algorithm popularized by Cooley and Tukey’s landmark paper (1965). Immediately prior to the publication of that paper, nearly every DFT was calculated using an O(N2) algorithm. After the paper’s publication, the popularity of the DFT grew dramatically because of this new efficient class of algorithms.

The conventional signal application requires high computational power based on Fast Fourier Transform (FFT) in addition to the ability to choose the algorithm and architecture. When considering alternate FFT algorithm analysis the criteria to consider are: execution speed, programming effort, hardware design effort, system cost, flexibility and precision. Nevertheless, for real time signal processing the main concern is execution speed.

The FFT Algorithm

As a fast computation algorithm, compared to DFT, the Fast Fourier Transform(FFT) is famous for decomposing the DFT computing module into small calculation blocks, which is called radix-2. By using that, the arithmetical complexity will be decreased from $O(N_2)$ to $O(Nlog_2N)$, which will increase the computation speed and the total computational cost will be greatly reduced.

Before using the radix-2 algorithm, the hardware realization of the 32- point FFT is parallel-in parallel-out, which is inappropriate for the analysis, because of the large amount of the usage of the adders and the multipliers.

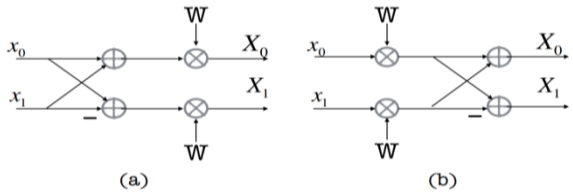

Fig. 1.1: The positions of twiddle factors in (a) radix-2 DIF butterfly and (b) radix-2 DIT butterfly

The number of the input ports for the whole architecture is more than 32 ports, i.e. for the chip manufacturing, the pins of the chip would increase at the same time.

Typically, the multiplication coefficients algorithms are called twiddle factors. For the FFT algorithm that has been used in this study a radix-2 DIF butterfly configuration is used.

Another configuration corresponding to the previous one is radix-2 DIT butterfly, the di difference between these two algorithms is the location of the twiddle factors. Fig. 1.1 illustrates the different position of the twiddle factors respectively.

The 4-point FFT

The input signals are in sequence order; on the contrary, the output signals are bit-reversed. During the procedure of analysis in hardware, the output signals are reorganized to bit sequence order. The 4 - point DIF FFT data-flow graph.

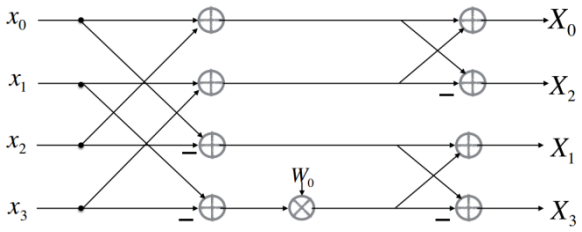

Fig. 1.2: A flow graph of the complex valued 4-point radix-2 DIF FFT Algorithm

The output values of X0, X1, X2, X3, which can be seen in the fig. 1.2 are as described.

$$X_0(k) = x_0 + x_2 + x_1 + x_3$$

$$X_1(k) = x_0 - x_2 + j(x_1 - x_3)$$

$$X_2(k) = x_0 + x_2 - x_1 - x_3$$

$$X_3(k) = x_0 - x_2 - j(x_1 - x_3)$$

The DFT Algorithm

The DFT is short for Discrete Fourier Transform, which is one of the most crucial algorithms that have been used in digital signal processing and image processing industries.

The DFT algorithm is defined in below given equation, where n is an element belongs to a matrix row; k represents row, which equals to 0 to N-1.

$$X(k) = \sum_{n=0}^{N-1} s(n) W_N^{kn}$$

$$W_N^{kn} = e^{\frac{-j2\pi kn}{N}}$$

The magnitude and phase of the DFT algorithm are described in equation as below:

$$Mag\,(X(k)) = \sqrt[2]{X_R e(k)^2 + X_I m(k)^2}$$

$$\varphi(X(k)) = \arctan \frac{X_I m(k)}{X_{Re} e(k)}$$

In order to reduce the computation complexity of DFT algorithm, some changes have been added to the algorithm, in terms of convenience and efficiency.

II. LITERATURE SURVEY

SR. NO.	TITLE	AUTHORS	YEAR	METHODOLOGY
1	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	A. X. Glittas, M. Sellathurai and G. Lakshminarayanan	June 2016	This paper presents a novel pipelined FFT processor for the FFT computation of two independent data streams.
2	A new approach to pipeline FFT processor	Shousheng He and M. Torkelson	1996	A new VLSI architecture for a real-time pipeline FFT processor is proposed.
3	A 2.4-Gsample/s DVFS FFT Processor for MIMO OFDM Communication Systems	Y. Chen, Y. W. Lin, Y. C. Tsao and C. Y. Lee	May 2008	This paper presents a new dynamic voltage and frequency scaling (DVFS) FFT processor for MIMO OFDM applications.
4	An Area- and Energy-Efficient Multimode FFT Processor for WPAN/WLAN/WMAN Systems	S. N. Tang, C. H. Liao and T. Y. Chang	June 2012	This paper presents a multimode FFT processor for wireless personal area network (WPAN), wireless local area network (WLAN), and wireless metropolitan area network (WMAN) applications.
5	A reconfigurable FFT architecture for variable-length and multi-streaming OFDM standards	P. P. Boopal, M. Garrido and O. Gustafsson	2013	This paper presents a reconfigurable FFT architecture for variable-length and multi-streaming WiMax wireless standard and The proposed architecture has been synthesized for the Virtex-6 XCVLX760 FPGA.
6	MDC FFT/IFFT Processor With Variable Length for MIMO-OFDM Systems	K. J. Yang, S. H. Tsai and G. C. H. Chuang	April 2013	This paper presents an multipath delay commutator (MDC)-based architecture and memory scheduling to implement fast Fourier transform (FFT) processors

A. X. Glittas, M. Sellathurai and G. Lakshminarayanan,[1] Nowadays, many applications require simultaneous computation of multiple independent fast Fourier transform (FFT) operations with their outputs in natural order. Therefore, this brief presents a novel pipelined FFT processor for the FFT computation of two independent data streams. The proposed architecture is based on the multipath delay commutator FFT architecture. It has N/2-point decimation in time FFT and N/2-point decimation in frequency FFT to process the odd and even samples of two data streams separately. The main feature of the architecture is that the bit reversal operation is performed by the architecture itself, so the outputs are generated in normal order without any dedicated bit reversal circuit. The bit reversal operation is performed by the shift registers in the FFT architecture by interleaving the data. Therefore, the proposed architecture requires a lower number of registers and has high throughput.

Shousheng He and M. Torkelson, [2] A new VLSI architecture for a real-time pipeline FFT processor is proposed. A hardware-oriented radix-22 algorithm is derived by integrating a twiddle factor decomposition technique in the divide-and-conquer approach. The radix-22 algorithm has the same multiplicative complexity as the radix-4 algorithm, but retains the butterfly structure of the radix-2 algorithm. The single-path delay-feedback architecture is used to exploit the spatial regularity in the signal flow graph of the algorithm. For length-N DFT computation, the hardware requirement of the proposed architecture is minimal on both dominant components: log4N-1 complexity multipliers and N-1 complexity data memory. The validity and efficiency of the architecture have been verified by simulation in the hardware description language VHDL.

Y. Chen, Y. W. Lin, Y. C. Tsao and C. Y. Lee, [3] This paper presents a new dynamic voltage and frequency scaling (DVFS) FFT processor for MIMO OFDM applications. By the proposed multimode multipath-delay-feedback (MMDF) architecture, our FFT processor can process 1-8-stream 256-point FFTs or a high-speed 256-point FFT in two processing domains at minimum clock frequency for DVFS operations. A parallelized radix-24 FFT algorithm is also employed to save the power consumption and hardware cost of complex multipliers. Furthermore, novel open-loop voltage detection and scaling (OLVDS) mechanism is proposed for fast and robust voltage management. With these schemes, the proposed FFT processor can operate at adequate voltage/frequency under different configurations to support the power-aware feature. A test chip of the proposed FFT processor has been fabricated using UMC 90 nm single-poly nine-metal CMOS process with a core area of 1.88 times1.88 mm2 . The SQNR performance of this FFT chip is over 35.8 dB for QPSK/16-QAM modulation. Power dissipation of 2.4 Gsample/s 256-point FFT computations is about 119.7 mW at 0.85 V. Depending on the operation mode, power can be saved by 18%-43% with voltage scaling in TT corner.

S. N. Tang, C. H. Liao and T. Y. Chang, [4] this paper presents a multimode FFT processor for wireless personal area network (WPAN), wireless local area network (WLAN), and wireless metropolitan area network (WMAN) applications. Using the proposed flexible-radix-configuration multipath-delay-feedback (FRCMDF) architecture, variable-length/multiple-stream FFTs capable of achieving a high throughput can be performed in a hardware-efficient manner. Based on the FRCMDF structure, a dual-optimized multiplication scheme is also proposed to further improve the area and energy efficiency. In addition, the proposed configuration scheme can provide an architectural support for power scalability across FFT modes. A test chip for the proposed FFT processor has been designed and fabricated using a TSMC-0.18 m CMOS process with a core size of 3.2 mm^2 and a signal-to-quantization-noise ratio (SQNR) of over 40 dB. When the FFT mode is configured to operate as a 2.4 GS/s 512-point FFT at 300 MHz, the measured power consumption is 507 mW. Compared with previous multimode FFT designs, our FFT chip is more area- and energy-efficient as it is able to provide relatively higher throughput per unit area or per unit power consumption. Also, the power scalability across FFT modes is relatively exhibited in the proposed FFT processor.

P. P. Boopal, M. Garrido and O. Gustafsson,[5] This paper presents a reconfigurable FFT architecture for variable-length and multi-streaming WiMax wireless standard. The architecture processes 1 stream of 2048-point FFT, up to 2 streams of 1024-point FFT or up to 4 streams of 512-point FFT. The architecture consists of a modified radix-2 single delay feedback (SDF) FFT. The sampling frequency of the system is varied in accordance with the FFT length. The latch-free clock gating technique is used to reduce power consumption. The proposed architecture has been synthesized for the Virtex-6 XCVLX760 FPGA. Experimental results show that the architecture achieves the throughput that is required by the WiMax standard and the design has additional features compared to the previous approaches. The design uses 1% of the total available FPGA resources and maximum clock frequency of 313.67 MHz is achieved. Furthermore, this architecture can be expanded to suit other wireless standards.

K. J. Yang, S. H. Tsai and G. C. H. Chuang, [6] This paper presents an multipath delay commutator (MDC)-based architecture and memory scheduling to implement fast Fourier transform (FFT) processors for multiple input multiple output-orthogonal frequency division multiplexing (MIMO-OFDM) systems with variable

length. Based on the MDC architecture, authors propose to use radix- Ns butterflies at each stage, where Ns is the number of data streams, so that there is only one butterfly needed in each stage. Consequently, a 100% utilization rate in computational elements is achieved. Moreover, thanks to the simple control mechanism of the MDC, authors propose simple memory scheduling methods for input data and output bit/set-reversing, which again results in a full utilization rate in memory usage. Since the memory requirements usually dominate the die area of FFT/inverse fast Fourier transform (IFFT) processors, the proposed scheme can effectively reduce the memory size and thus the die area as well. Furthermore, to apply the proposed scheme in practical applications, authors let Ns=4 and implement a 4-stream FFT/IFFT processor with variable length including 2048, 1024, 512, and 128 for MIMO-OFDM systems. This processor can be used in IEEE 802.16 WiMAX and 3GPP long term evolution applications. The processor was implemented with an UMC 90-nm CMOS technology with a core area of 3.1mm2. The power consumption at 40 MHz was 63.72/62.92/57.51/51.69 mW for 2048/1024/512/128-FFT, respectively in the post-layout simulation. Finally, authors analyse the complexity and performance of the implemented processor and compare it with other processors. The results show advantages of the proposed scheme in terms of area and power consumption.

III. PROBLEM IDENTIFICATION

This brief has presented a novel FFT processor whose outputs are generated in the natural order. The proposed processor can process two independent data streams simultaneously, and makes it suitable for many high-speed real-time applications. The bit reversal circuit present in prior designs is eliminated by integrating two FFT processors and the registers, which are present in the architectureare reused for bit reversal. As a result, the need of additional registers to bit reverse the outputs is avoided. Moreover, the proposed architecture provides throughput higher than the prior architectures. These attributes makes system more complex.

IV. CONCLUSION

The fast Fourier transforms (FFT) and discrete Fourier transform (DFT) is used to deliver a fast approach for the processing of data in the wireless transmission. These are the fundamental mathematical operations used in digital signal processing. It allows the user to analyse, modify, and synthesize signals in a digital environment. Because of this, it has found a wide range of uses in engineering and scientific applications. The Fast Fourier Transform is one of the methods of converting the time domain data to frequency domain data with less hardware requirement and fast time utilization.

REFERENCES

[1] A. X. Glittas, M. Sellathurai and G. Lakshminarayanan, "A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 6, pp. 2402-2406, June 2016.

[2] Shousheng He and M. Torkelson, "A new approach to pipeline FFT processor," Parallel Processing Symposium, 1996., Proceedings of IPPS '96, The 10th International, Honolulu, HI, , pp. 766-770, 1996.

[3] Y. Chen, Y. W. Lin, Y. C. Tsao and C. Y. Lee, "A 2.4-Gsample/s DVFS FFT Processor for MIMO OFDM Communication Systems," in IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1260-1273, May 2008.

[4] S. N. Tang, C. H. Liao and T. Y. Chang, "An Area- and Energy-Efficient Multimode FFT Processor for WPAN/WLAN/WMAN Systems," in IEEE Journal of Solid-State Circuits, vol. 47, no. 6, pp. 1419-1435, June 2012.

[5] P. P. Boopal, M. Garrido and O. Gustafsson, "A reconfigurable FFT architecture for variable-length and multi-streaming OFDM standards," 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013), Beijing, pp. 2066-2070, 2013.

[6] K. J. Yang, S. H. Tsai and G. C. H. Chuang, "MDC FFT/IFFT Processor With Variable Length for MIMO-OFDM Systems," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 4, pp. 720-731, April 2013.

[7] M. Ayinala, M. Brown, and K. K. Parhi, “Pipelined parallel FFT architectures via folding transformation,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 6, pp. 1068–1081, Jun. 2012.

[8] M. Garrido, J. Grajal, and O. Gustafsson, “Optimum circuits for bit reversal,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 10, pp. 657–661, Oct. 2011.

[9] S.-G. Chen, S.-J.Huang, M. Garrido, and S.-J.Jou, “Continuous-flow parallel bit-reversal circuit for MDF and MDC FFT architectures,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 10, pp. 2869–2877, Oct. 2014.

[10] M. Garrido, J. Grajal, M. A. Sanchez, and O. Gustafsson, “Pipelined radix-2k feedforward FFT architectures,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 1, pp. 23–32, Jan. 2013.

[11] Z. Wang, X. Liu, B. He, and F. Yu, “A combined SDC-SDF architecture for normal I/O pipelined radix-2 FFT,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 5, pp. 973–977, May 2015.

[12] A. X. Glittas and G. Lakshminarayanan, “Pipelined FFT architectures for real-time signal processing and wireless communication applications,” in Proc. 18th Int. Symp. VLSI Design Test, Jul. 2014, pp. 1–2.

[13] Y.-N. Chang, “An efficient VLSI architecture for normal I/O order pipeline FFT design,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 12, pp. 1234–1238, Dec. 2008.