An Aging-Aware Reliable Multiplier Design: A Survey

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Abstract: ***Negative Bias Temperature Instability (NBTI) in silicon based metal-oxide semiconductor-field-effect-transistors (MOSFETs) has been recognized as a critical reliability issue for advanced space qualified electronics. The phenomenon manifests itself as a modification of threshold voltage (V^{th}) resulting in degraded signal timing paths, and ultimately circuit failure. Despite the obvious importance of the issue, a standard measurement protocol has yet to be determined. This is a consequence of a large amount of complexity introduced by the strong dependencies of NBTI on temperature, electric field, frequency, duty cycle, and gate dielectric composition. Indeed, researchers are nowhere near a dependable circuit reliability lifetime predictor formula that would be accurate among a wide variety of technology specifications.***

Keywords— Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

I. INTRODUCTION

Aging variations refer to the temporal variations in delay of the underlying devices and circuits in a chip. The primary on-chip aging mechanisms, that affect CMOS devices, can be classified into several categories, outlined below. Since it is considered to be the primary source of aging induced delays shifts in digital circuits.

Bias Temperature Instability (BTI):

Negative/positive bias temperature instability (NBTI/PBTI) in PMOS/NMOS devices is collectively referred to as BTI. In a CMOS device, when a PMOS (NMOS) is stressed under BTI, typically by applying a logic 0 (logic 1) at its gate input, its threshold voltage degrades, resulting in an increase in the delay of the device. When the stress is removed, there is partial (but not complete) recovery in the threshold voltage, and hence the delay degradation is also partially ameliorated.

Hot Carrier Injection (HCI):

When a carrier (electron/hole) in the channel of a CMOS device gains sufficient kinetic energy (becomes hot), it can get injected into the gate dielectric and cause interface trapsto be generated. This results in a Vth shift of the device, and hence, degradation of delay and other switching properties over time.

Time Dependent Dielectric Breakdown (TDDB):

Oxide breakdown refers to the creation of a current path from the gate to thechannel, and thishappens due to the generation of defects in SiO2 gate oxide, when stress is applied over a long period of time. When the defect density reaches a critical value, a conductive path is formed through the oxide, resulting in a functional failure of the device.

Bias Temperature Instability

Bias temperature instability refers to the instability created in the bonding structure at the substrate-oxide interface of the CMOS device, when a bias (stress) is applied to the gate terminal with respect to the source terminal. In PMOS, the application of a zero/negative VG voltage creates a negative bias at the gate terminal with respect to the source, as shown in Fig. 1.1. When logic 1 is applied, the relative bias between the gate and source terminals becomes zero. The application of negative bias, either for a long period of time or in conjunction with alternating zero biases, can cause the PMOS to age with time, or suffer from delay degradation.

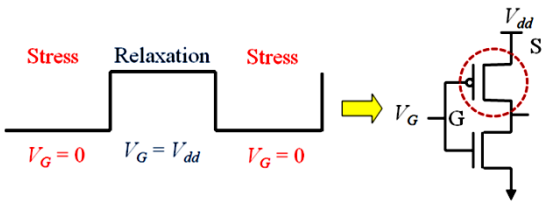

Figure 1.1: digital signal to the gate terminal of the CMOS

VHDL

An entity declaration, or entity, combined with architecture or body constitutes a VHDL model. VHDL calls the entity-architecture pair a design entity. By describing alternative architectures for an entity, we may configure a VHDL model for a specific level of investigation. The entity contains the interface description common to the alternativearchitectures. It communicates with other entities and the environment through ports andgenerics. Generic information particularizes an entity by specifying environment constants such as register size or delay value. For example,

```
e ntityA is
        port (x, y: in real; z: out real);
        gen e ric (d e lay: time);
endA;
```

The architectur e contains declarativ e and statem e nt s e ctions. D e clarations form the r e gion befor e the reserv e d word b e gin and can declar e local elem e nts such as signals and compon e nts. Statem e nts app e ar aft e r *b e gin* and can contain concurr e nt statem e nts. For instanc e ,

```
architectur e  B of A is
        compon e nt M
        port ( j : in r e al ; k : out real);
        end compon e nt;
signala,b,c r e al := 0.0;
b e gin
        "concurr e nt statem e nts"
end B;
```

The variety of concurrent statement types gives VHDL the descriptive power to create and combine models at the structural, dataflow, and behavioral levels into one simulation model. The structural type of description makes use of component instantiation statements to invoke models described elsewhere. After declaring components, use them in the component instantiation statement, assigning ports to local signals or other ports and giving values to generics. invert: M port map (j => a ; k => c); Then bind the components to other design entities through configuration specifications in VHDL's architecture declarative through separate configuration declarations.

The dataflow style makes wide use of a number of types of concurrent signal assignment statements, which associate a target signal with an expression and a delay. The list of signals appearing in the expression is the sensitivity list; the expression must be evaluated for any change on any of these signals. The target signals obtain new values after the delay specified in the signal assignment statement. If no delay is specified, the signal assignment occurs during the next simulation cycle:

```
c <= a + b after delay;
```

VHDL also includes conditional and selected signal assignment statements. It uses block statements to group signal assignment statements and makes them synchronous with a guarded condition. Block statements can also contain ports and generics to provide more modularity in the descriptions. Commonly use concurrent process statements whenwe wish to describe hardware at the behavioral level of abstraction. The processstatement consists of declarations and procedural types of statements that make up the sequential program. Wait and assert statements add to the descriptive power of the process statements for modeling concurrent actions:

```
proc e ss
b e gin
        variabl e  i : r e al := 1.0;
wait on a;
        i = b * 3.0;
        c <= i aft e r d e lay;
end proc e ss;
```

Other concurrent statements include the concurrent assertion statement, concurrent procedure call, and generate statement. Packages are design units that permit types and objects to be shared. Arithmetic operations dominate the execution time of most Digital Signal Processing (DSP) algorithms and currently the time it takes to execute a multiplication operation is still the dominating factor in determining the instruction cycle time of a DSP chip and Reduced Instruction Set Computers (RISC). Among the many methods of implementing high speed parallel multipliers, there is one basic approach namely Booth algorithm.

II. SYSTEM MODEL

NBTI

Negative Bias Temperature Instability (NBTI) has emerged as a major reliability challenge for the semiconductor industry in recent years. NBTI impact is getting worse in each technology generation with greater performance and reliability loss. When a negative voltage is applied at a p channel transistor (PMOS) gate, interface traps are formed near oxide layer, causing a change in transistor characteristics. When the input to a PMOS is low (logic zero), the transistor is in a stress phase. During the stress phase, the transistor parameters slowly deviate from the nominal value. When the input to the PMOS is high (logic one), the transistor is in a recovery phase. During the recovery phase, trapped charges are released, regaining the original transistor state. The PMOS enters into stress and recovery phases alternately, when the input to the PMOS is dynamic. Longer the stress period, higher is the impact of NBTI on transistor parameters. Therefore, input to the transistor indirectly determines the extent of NBTI degradation.

The Reaction Diffusion Model

The original Reaction Diffusion (RD) model for NBTI was undoubtedly the simplest case scenario. It involved only a single mechanism which resulted in the creation of an interface state, similar to those created in hot carrier

injection. In this model a hole from the inversion channel, in the presence of a vertical electric field induced by the surface potential, is attracted to the semiconductor/insulator interface where it interacts with Si-H bonds created during passivation of the dangling Si bonds at the interface. This interaction was believed to weaken the Si-H bond to the point that it would break. At elevated temperature the Si-H bonds dissociate and subsequently the neutral atomic hydrogen captures a hole and becomes positively charged.

Two Stage Model

A more elaborated multi-mechanism explanation is the two stage model proposed by T. Grasser, et al [9]. In this theory the precursor for the phenomenon is a neutral interfacial oxygen vacancy, which upon the capture a hole, creates a positive defect called an E′γ center. Next, the emission of a hole (electron capture) neutralizes the defect at which point the structure can either relax back to the original oxygen vacancy precursor, or re-capture a hole and return to the E′γ state.

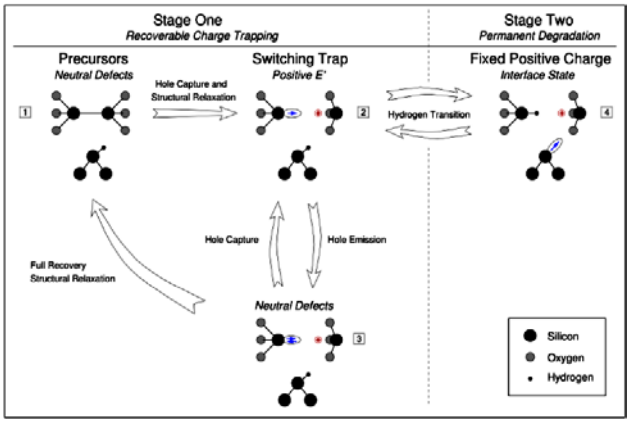

Figure 1.2 Two stage model

This is the mechanism believed to account for the rapid charging and recovery dynamics observed in NBTI. As for the second mechanism, the E′γ center can interact with the hydrogen passivation a neighboring silicon dangling bond at the interface. Simple thermodynamic arguments [10] show that it is energetically favorable for the hydrogen to migrate to the E′γ center leaving behind an interface state whose charge will depend on the position of the Fermi level. An illustration of this mechanism is shown in Fig.1.2.

III. LITERATURE SURVEY

C. Lin, Y. H. Cho and Y. M. Yang, [1] Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = -Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this research, authors propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column or row-bypassing multiplier. The experimental results show that their proposed architecture with 16 × 16 and 32 × 32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column-bypassing multipliers. Furthermore, their proposed architecture with 16 × 16 and 32 × 32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement as compared with 16×16 and 32 × 32 fixed-latency row-bypassing multipliers.

S. Zafar et al.,[2] Threshold voltage (Vt) of a field effect transistor (FET) is observed to shift with stressing time and this stress induced V t shift is an important transistor reliability issue. Vt shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping. In this research, authors present a comparative study of NBTI and PBTI for a variety of FETs with different dielectric stacks and gate materials. The study has two parts. In part I, NBTI and PBTI measurements are performed for FUSI NiSi gated FETs with SiO2 SiO2/HfO2 and SiO2/HfSiO as gate dielectric stacks and the results are compared with those for conventional SiON/poly-Si FETs. The main results are: (i) NBTI for SiO 2/NiSi and SiO2/HfO2/NiSi are same as those conventional SiON/poly-Si FETs; (ii) PBTI significantly increases as the Hf content in the high K layer is increased; and (iii) PBTI is a greater reliability issue than NBTI for HfO2/NiSi FETs. In part II of the study, NBTI and PBTI measurements are performed for SiO2/HfO2 devices with TiN and Re as gates and the results are compared with those for NiSi gated FETs. The main results are: (i) NBTI for SiO 2/HfO2/TiN and SiO2/HfO2/Re pFETs are similar with those observed for NiSi gated pFETs; and (ii) PBTI inTiN and Re gated HfO2 devices is much smaller than those observed for SiO2/HfO2/NiSi. In summary for SiO2/HfO2 stacks, NBTI is observed to be independent of gate material whereas PBTI is significantly worse for FUSI gated devices. Consequently, HfO2 FETs with TiN and Re gates exhibit over all superior transistor reliability characteristics in comparison to HfO2/FUSI FETs.

S. Zafar, A. Kumar, E. Gusev and E. Cartier,[3] Over recent years, there has been increasing research and

development efforts to replace SiO2 with high dielectric constant (high-κ) materials such as HfO2, HfSiO, and Al2O3. An important transistor reliability issue is the threshold voltage stability under prolonged stressing. In these materials, threshold voltage is observed to shift with stressing time and conditions, thereby giving rise to threshold voltage instabilities. In this research, authors review various causes of threshold voltage instability: charge trapping under positive bias stressing, positive charge creation under negative bias stressing (NBTI), hot-carrier stressing, de-trapping and transient charge trapping effects in high-κ gate dielectric stacks. Experimental and modeling studies for these threshold voltage instabilities are reviewed.

H. I. Yang, S. C. Yang, W. Hwang and C. T. Chuang,[4] Negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) weaken PFET and NFET over the lifetime of usage, leading to performance and reliability degradation of nanoscale CMOS SRAM. In addition, most of the state-of-the-art SRAM designs employ replica timing control circuit to mitigate the effects of leakage and process variation, optimize the performance, and reduce power consumption. NBTI and PBTI also degrade the timing control circuits and may render them ineffective. In this research, authors provide comprehensive analyses on the impacts of NBTI and PBTI on a two-port 8T SRAM design, including the stability and Write margin of the cell, Read/Write access paths, and replica timing control circuits. Authors show, for the first time, that because the Read/Write replica timing control circuits are activated in every Read/Write cycle, they exhibit distinctively different degradation behavior from the normal array access paths, resulting in degradation of timing control and performance. Authors also discuss degradation tolerant design techniques to mitigate the performance and reliability degradation induced by NBTI/PBTI.

R. Vattikonda, Wenping Wang and Yu Cao, [5] Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this research, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robust design solutions: (1) the most effective techniques to mitigate the NBTI degradation are VDD tuning, PMOS sizing, and reducing the duty cycle; (2) an optimal VDD exists to minimize the degradation of circuit performance; (3) tuning gate length or the switching frequency has little impact on the NBTI effect; (4) a new switching scenario is identified for worst case timing analysis during NBTI stress.

IV.PROBLEM IDENTIFICATION

An aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that previous proposed architecture with 16× 16 and 32× 32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance compared with the 16 × 16 and 32 × 32 FLCB multipliers, respectively. Electro migration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, Electromigration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences.

V. CONCLUSION

Multipliers are one the most important component of many systems. So we always need to find a better solution in case of multipliers. Our multipliers should always consume less power and cover less power. So through our project we try to determine which of the three algorithms works the best. In the end we studied that radix 4 modified booth algorithm works the best. The aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, variable latency multipliers may be used under the influence of both the BTI effect and electro migration. In addition, variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period.

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