Review on Multichannel AMBA AHB with Multiple Arbitration Technique

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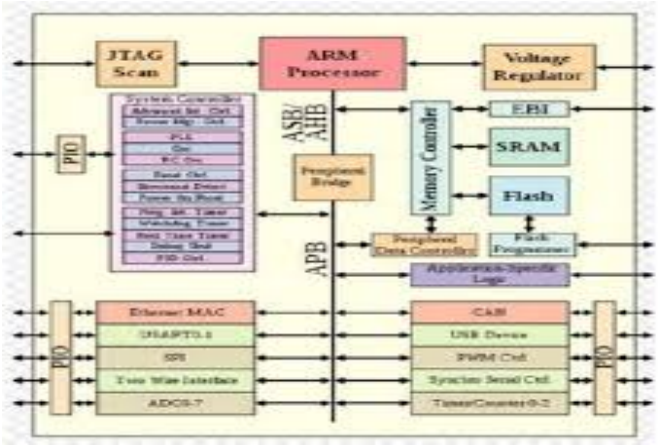
Abstract - Multiprocessor SOC designs have more than one processor and huge memory on chip. Soc uses both hardware and software processor. Multiple component like DSP, application based components, logics CPU etc. The components are integrated to form heterogeneous circuit .To perform efficiently it need system bus with high bandwidth which can process multiple signal in parallel. So system bus plays key role for data transfer and efficient communication. High performance buses available currently are from silicore, IBM, ARM. Advanced microcontroller bus architecture (AMBA) is protocol that is used as open standard on chip interconnection and management of functional blocks in system on chip. With combination of high performance on chip buses such as AMBA bus, we can solve bandwidth related problems. ARM uses ARB bus matrix and due to simple design and more flexibility in design uses mostly in SOC designs. AMBA bus having excellent architecture, at the same time power consumption is very less. Here we want to use four variables to develop multiple option, we will use round robin and fixed priority by multiple arbitration technique. In that way we can increase speed of processor for efficient working.

Keywords – AMBA bus, Multiprocessor SOC, AHB, ARB.

1. INTRODUCTION

Integrated IC's uses thousands of Transistors and because of that circuit becomes very complex. Similarly Heterogeneous uses multiple devices with both programmed and non programmed type, again it lead to more complexity.



ARM SOC block (from ICCSP- 2014)

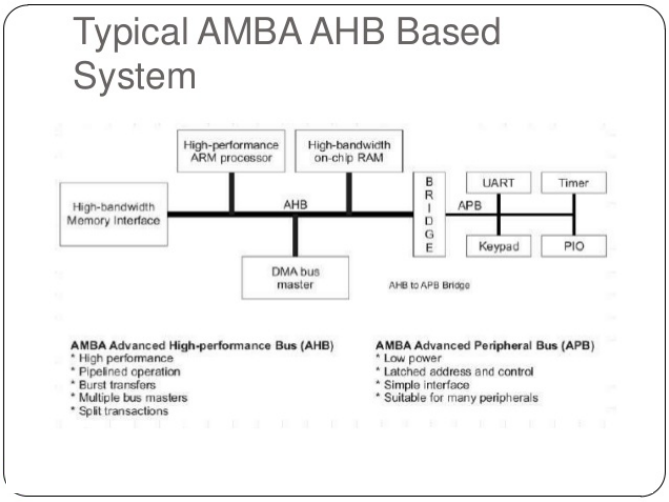
Modern system on chip contains master and slave modules. Master Modules are normally CPU, DMA, Graphics etc, slaves are memories, register and system on chip buses.SOC not only which components or blocks it uses but also interconnects.

AMBA is solution for different blocks to interface each other. AMBA specifications have been derived to satisfy four key requirements:-

1. To facilitate the right first time development of embedded microcontroller products with one or more CPUs or signal processors
2. To be technology independent and ensure that highly reusable peripheral and system macro cells can be migrated across a diverse range of IC processes and be appropriate for full custom, standard cell and Gate array technologies.
3. To encourage modular system design to improve processor independence providing a developed road map for advanced cache CPU and developed of peripheral libraries.
4. To minimize the silicon infrastructure required to support efficient on chip and off chip communication for both operation and manufacturing unit.

Different available buses are:-

1. Advanced high performance bus (AHB)
2. Advanced peripheral bus (APB)
3. Advanced System bus (ASB)



2. METHOD

We will use interconnect matrix for multichannel AMBA – AHB using multiple arbitration technique. Here we will use Master slave technology. Master will be CPU ,DMA etc .It can be multiple programmable device and slave will be register ,memories etc.

Master will send first requirement to access the bus. This request will be based on priority also. This priority can be round robin, fixed priority etc.

In dynamic arbitration once the command will execute priority of master will reduce by one.

In this project we will mix round robin and dynamic arbiter. Master will get access to bus only when round robin and dynamic arbiter give the grant signal.

In this section author should explain in little bit dept about his research or model he/she is working on. Author can be use suitable diagrams and images with the references mentioned [1] in square brackets from particular resource image or diagram author taken.

3. PREVIOUS WORK

Earlier , implemented the interconnect matrix for multichannel AMBA-AHB using multiple arbitration technique. The design of arbiter for flexible bus matrix supports the priority policy as round robin, fixed priority, dynamic arbitration. In round robin arbitration mechanism, the arbiter gives accesses to the bus depending upon master's request. The master who sends first request to the arbiter gets first access to the bus. In fixed priority, the priority of all master are fixed. So, a master gets access to the bus depending upon priority. The dynamic arbitration mechanism also depends upon priority. But, in this after getting access to the bus the priority of master reduces by 1. In new arbiter, they combined the round robin and dynamic arbiter. In this, master's gets access to the bus only when round robin and dynamic arbiter gives the grant signal. As per requirement we can use any one mechanism.

4. DISCUSSION

Reference taken from base paper International conference on communication and signal processing April 3-5 ,2014 , they have chosen some parameters and have demonstrated lookup table ,where area speed and power consumption comes in picture.

We are working up to 4 master implementation and can go up to 16 masters and can make split capable.

5. FUTURE SCOPES

We are working up to 4 master implementation and can go up to 16 masters and can make split capable.

In that way we can design very efficient system with faster speed less power consumption and will take care of all priorities.

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