To Improve Noise by increasing the Output current for Dynamic CMOS Logic with Stack Techniques

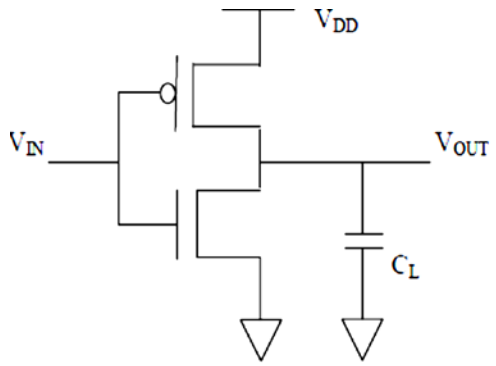
Mayura Upasani[1],Sachin Bandewar[2]

Abstract:-The most common way to decrease noise is to add one or more stack transistors to the system. This decreases charge sharing and charge leakage problem and thus decreases noise problem. Stack transistors or transistor stacking has proven to be exceedingly most effective in reducing and minimizing sub threshold leakage or charge leakage in standby mode of operation of circuit. It has been observed that this technique of using stack transistors saves around 33% in total leakage in 50nm devices. Dynamic CMOS circuits are extensively used in high performance Very Large Scale Integrated systems (VLSI). Conversely they undergo commencing limitations like noise tolerance, charge leakage, charge sharing, delay etc. Because of growing impact of process variations on design performance, belligerent technology scaling noise in dynamic CMOS has become than essential challenge. Noise is basically result of charge sharing problem and thus charge leakage problem. The noise stimulate in circuit would affect the performance of circuit, which should be so improved for reliable operation of VLSI systems.

Keywords: Micro wind 3.0.

I. INTRODUCTION

There are several techniques that reduce the rise time, fall time and output current or fan-out in efficient way but the disadvantage of each technique that limit the switching speed and fan-out. Due to this there are so many limitations are occurs. In this dissertation we had use stack techniques that can improved switching response and fan-out.

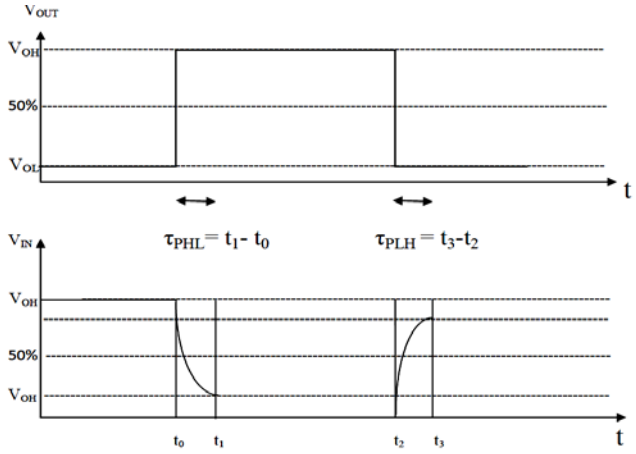


For the calculation of rise time, fall time and delay time of the any CMOS logic circuit we are using computer simulation as well as analytical techniques. Whenever we are using more complex CMOS logic circuit then we are considering appropriate transistor model for the simulation of Dynamic CMOS logic circuits.

The propagation delay tp of a gate defines how quickly it responds to a change at its inputs, it expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms as shown in the figure for an inverting gate.

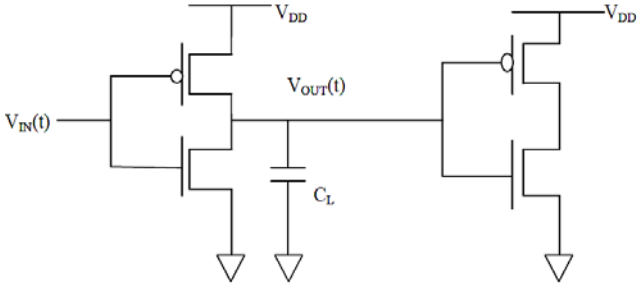
$$\tau p=(\tau pHL+ \tau pLH) / 2 \qquad \text{eq.(1)}$$

The τpHL defines the response time of the gate for a low to high output transition, while τpLH refers to a high to low transition. The propagation delay τp as the average of the two



1.1.1 Quick Design

We will give an example of how to calculate quick estimate. From Figure we can write following equations.



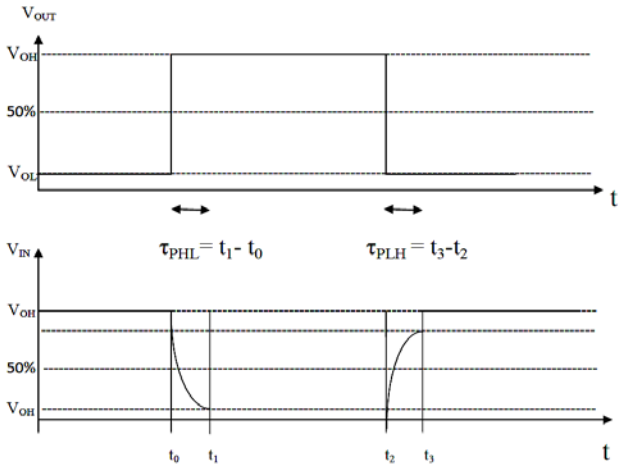
$V_{50\%} = V_{OL} + (V_{OH}-V_{OL})/2$

$V_{50\%}=(V_{OH}+V_{OL})/2$ eq. (2)

$V_{90\%} = V_{OL} + 0.9(V_{OH}-V_{OL})$ eq. (3)

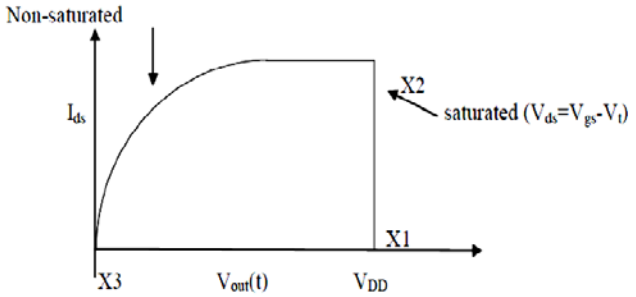
$V_{10\%} = V_{OL} + 0.1 (V_{OH}-V_{OL})$ eq. (4)

The τ_{pHL} defines the response time of the gate for a low to high output transition, while τ_{pLH} refers to a high to low transition. The propagation delay τ_p as the average of the two



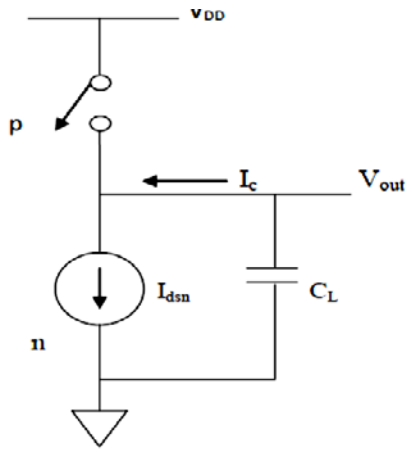
1.1.2 Rise and Fall Times

Figure shows the familiar CMOS inverter with a capacity load $\mathbf{C_L}$ that represents the load capacitance (input of next gates, output of this gate and routing) Of interest is the voltage waveform $\mathbf{V_{out}(t)}$ when the input is driven by a step waveform, $\mathbf{V_{in}(t)}$ as shown in figure

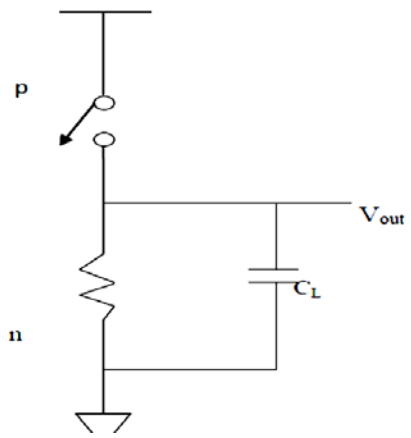


The equivalent circuits that illustrate the above behaviour are show in figure

Saturated : $V_{OUT} > V_{DD} - V_t$



Non-saturated : $0 < V_{OUT} < V_{DD} - V_{tn}$



Motivation

CMOS Technology was one of the main streams of VLSI Design. In 50nm and above technology switching speed is one of the main factors of system response. But when technology feature size shrinks switching speed create major issues. If we are design a small circuit with the help of CMOS design then switching speed cannot create major problem but when we are design a complex circuitry then switching speed cerate major problem.

For the solution of this problem we can used a technique that is called Stack technique. Through this we can improve the Switching speed or response of design circuitry. This technique is also used to reduce leakage current that can improve static power also.

Problem's Formulation

There are certain issues of process variations, timing, noise tolerance, and power which are looked into together for operation optimization [2]. We will use stack technique to improve following aspects:-

- Improve Rise time, Fall time, charge sharing, charge leakage problem in dynamic CMOS circuits.
- Optimize dynamic CMOS circuits with MOSFET-based keepers to enable and improve the rise time, fall time and output current etc, when we equate them to their initial performances.

Background Work

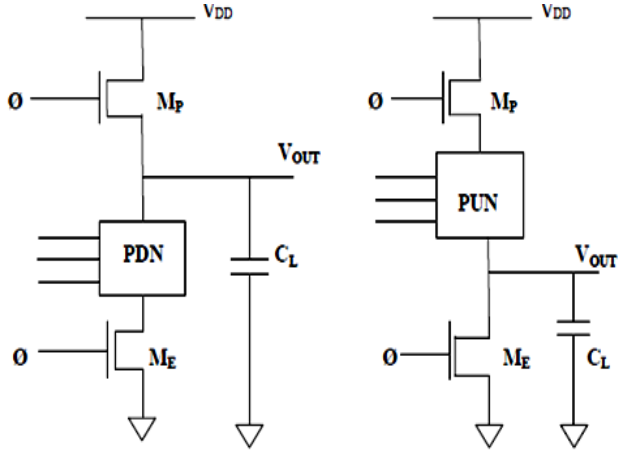
In this section we discussed the previous approaches which are nearly related to our research. Here we analyse previous technique that primarily target for reducing rise time, fall time and increasing fan-out. These techniques are shown in below. The approaches that are adopted in VLSI design. Hear we are using source voltage using NMOS, source voltage using PMOS, Feedback Keeper and Pre-charge internal nodes.

Methodology

The most common way to decrease noise is to add one or more stack transistors to the system[12]. This can solve rise time, fall time and fan-out problem. Using faster flip-flops decreases the setup (t_{su}) and hold times (V_{th}) of the flip-flop, which in change decreases the time window that the flip-flop is vulnerable to Noise. When the input frequency is less, the chances of the input turning during the setup and hold time studied for their optimization using the ac small-signal frequency-domain analysis. To date, simulations and ensuing analyses for the Noise problem have been performed mostly in the time domain. Designers of digital systems has time and again confronted with the problem of Noise. The problem could be rectified by the effective use of stack transistors.

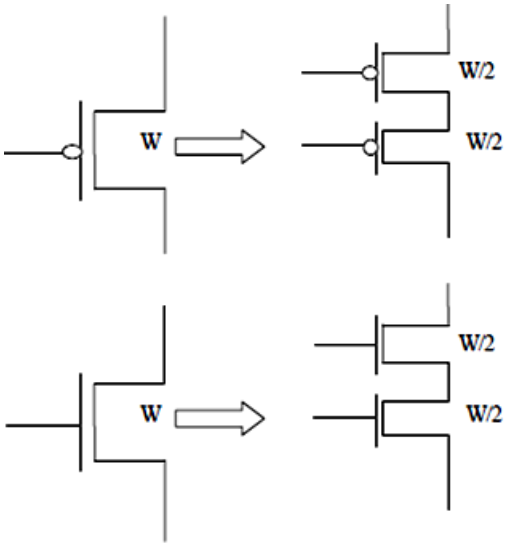
Dynamic Logic

In static logic families the pull up and pull down networks operate concurrently. Dynamic logic on the other hand uses a sequence of pre-charge and conditional evaluation phases which are controlled by the clock to realize complex logic functions. A dynamic logic block is shown in Figure. Both forms of Figure 4 can be used. In our analysis we will concentrate in Figure n-logic network. The operation of the pull-down network (PDN) can be divided into two major phases. The pre-charge and the evaluation phase. In what mode the circuit is operating is determined by the signal φ, the "clock" signal.

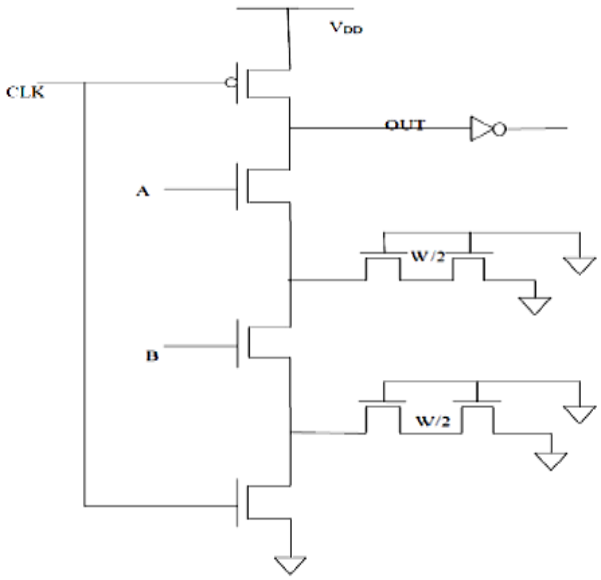


Propose Stack Method

In stack technique, MOS transistor is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, it induces reverse bias between them which results in the reduction of sub threshold leakage power. However, with increase in the number of transistors overall propagation delay of the circuit increases [12]. Using CMOS technology is basically for consuming less power. In this design criterion it focuses on sub threshold leakage power consumption and it also focuses on body biasing effect and stack effect. One of the main contributors for the static power consumption is sub threshold leakage current which is shown in the Figure i.e., the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink sub current is increases exponentially as the decrease of threshold voltage. Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power.



In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network often results in forged gate switching. A simple yet efficient way to avoid the charge leakage problem is to use stack of transistors in the pull-down network. An example dynamic 2-input AND gate using this technique is illustrated in Figure. In this width of stack of transistors is less than

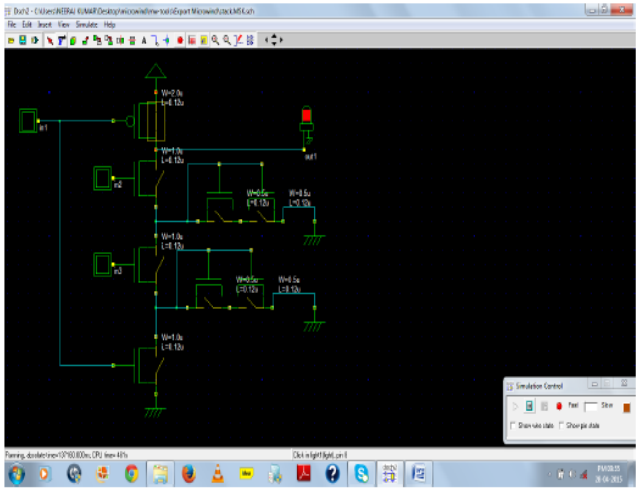


Working Principal

In working principal, we solve all 8 cases and give their output with designed circuit. Here we are using 7-NMOS (3-NMOS with W and 4-NMOS with W/2),1-PMOS,3-source voltage and 1-LED. In circuit diagram red colour indicate high voltage or 1, brown colour indicate hold circuit and blank colour indicate low voltage or 0.

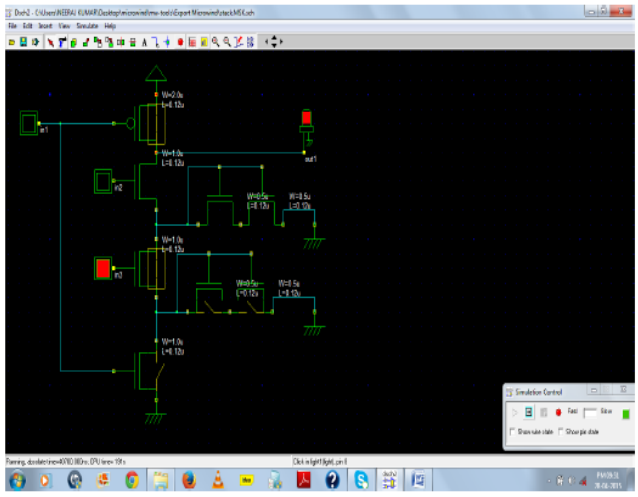
Case 1 :-

When we are taking CLK=0, A=0 and B=0 then circuit give high or 1 output



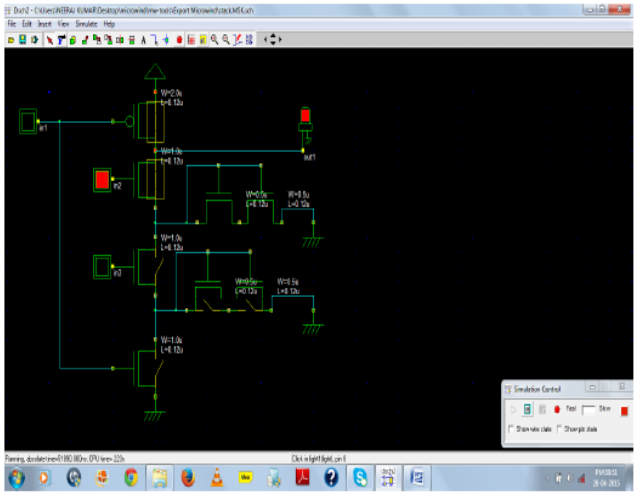
Case 2:-

When we are taking CLK=0, A=0 and B=1 then circuit give high or 1 output.



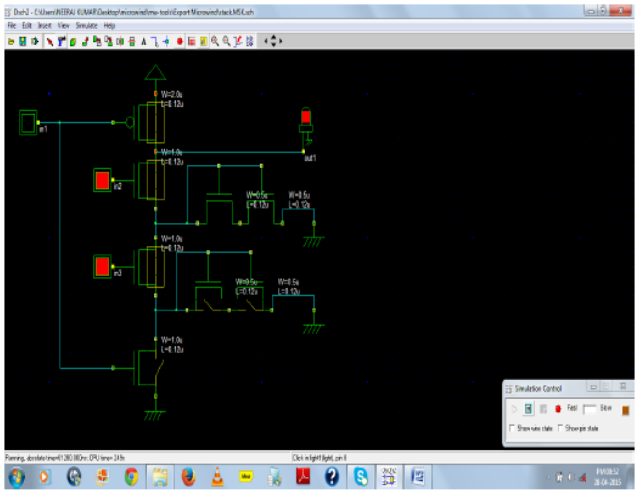
Case 3:-

When we are taking CLK=0, A=1 and B=1 then circuit give high or 1 output.



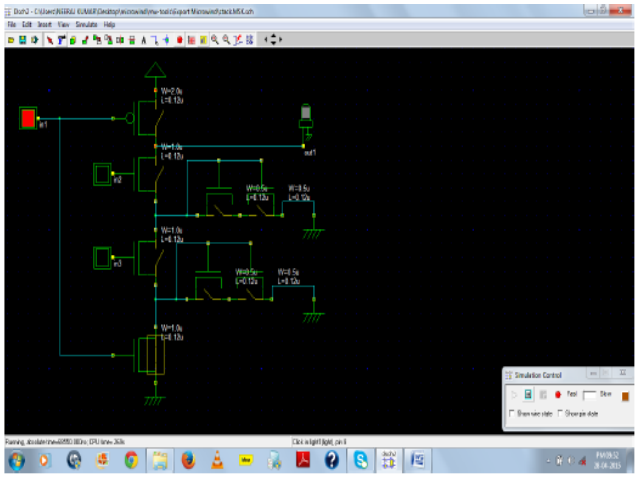
Case 4:-

When we are taking CLK=0, A=1 and B=1 then circuit give high or 1 output.



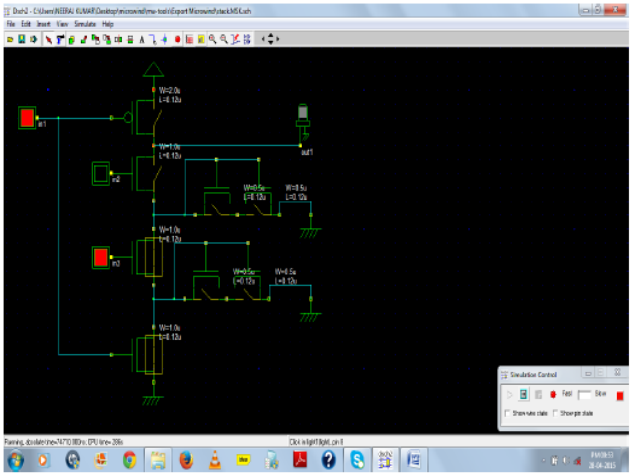
Case 5:-

When we are taking CLK=1, A=0 and B=0 then circuit is in hold mode.



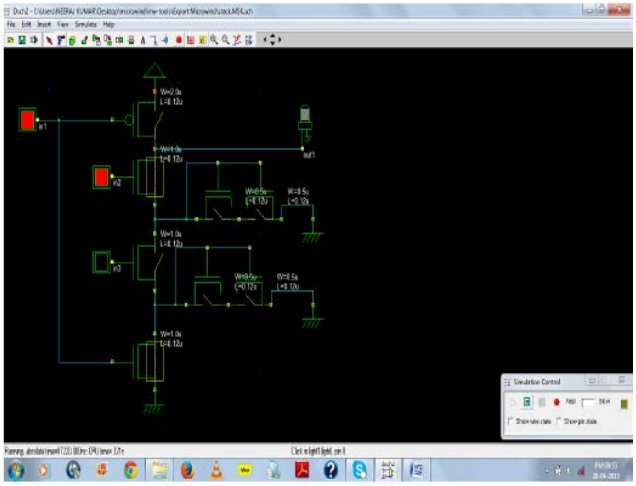
Case 6:-

When we are taking CLK=1, A=0 and B=1 then circuit is in hold mode.



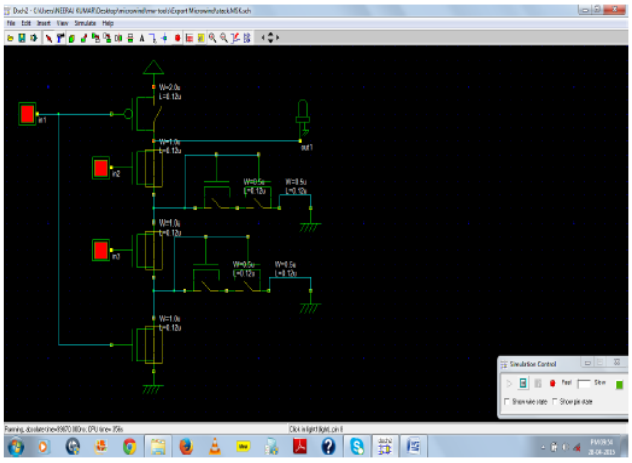
Case 7:-

When we are taking CLK=1, A=1 and B=0 then circuit is in hold mode.



Case 8:-

When we are taking CLK=1, A=1 and B=1 then circuit give high or 0 output.



Truth Table

CLK	A	B	O/P
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	Hold
1	0	1	Hold
1	1	0	Hold
1	1	1	0

FUNCTIONAL SIMULATION

4.1 Software Used

Software used For CMOS layout design is micro wind 3.0.

4.2 Microwind Layout

Integrated Circuit (IC) Layout or mask design is the description of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or implementation with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer‘s job is to place and connect all the components that make up a chip so that they meet all criteria. Typical goals are performance, size, and manufacturability. MICROWIND supports both front-end and back-end design flow. In order to design front-end, we use the Digital schematic editor i.e. DSCH which has simulator used for simulating digital circuits.

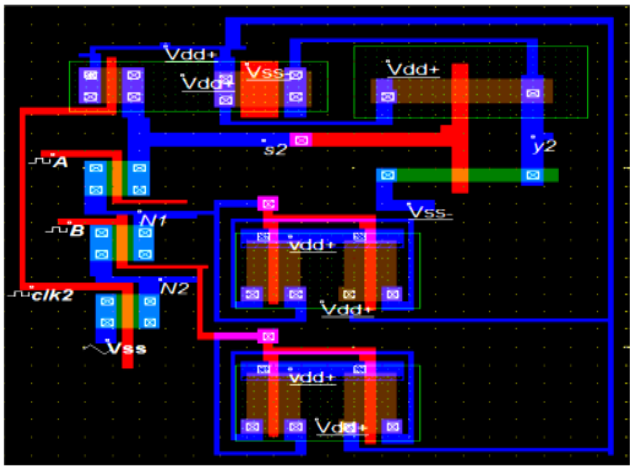
- MICROWIND generates an error free CMOS layout, and if any error occurs it reminds the user about the occurrence of error.
- Digital schematic editor could convert the digital circuits into Verilog file which may be moreover synthesized for FPGA/CPLD devices of any trafficker.
- Micro wind’s version 3 also supports the back end design.
- In distinguishable Verilog file is compiled for layout conversion in MICROWIND.
- In Micro wind, the CMOS layouts could be demonstrated using inbuilt mix-signal simulator and analyzed further for DRC, delays, 2D cross section, 3D view and etc.

4.2 (a) Layout of Propose Stack Method

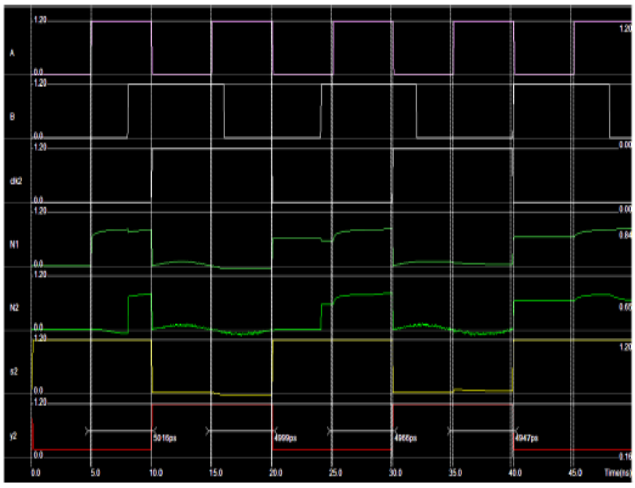
Firstly, we can draw propose stack circuit in DSCH screen. For this we can used 2-PMOS, 7-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, and connecting wire that can used to give proper connection. Through this we can design propose stack circuit. After the completion of design it save in MSK format. Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between:-

- Layout.
- Voltage Vs Time graph.
- Voltage Vs Current graph.
- Frequency and Time graph.

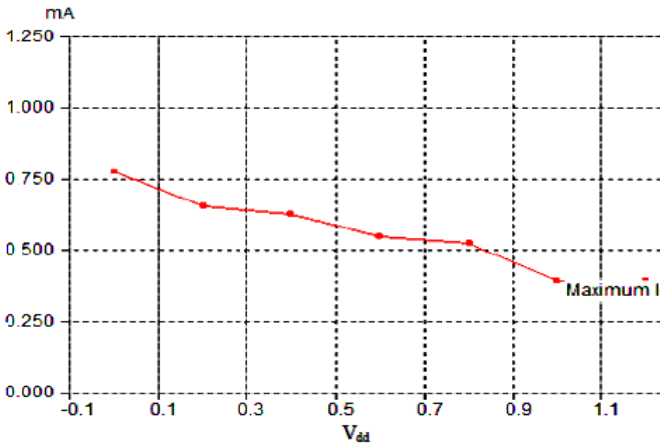
This is the layout of designed proposed method. This proposed circuit diagram is design in DSCH and layout is generated through microwimd. Here we are using microwind 3.0 software.



This is the simulation of proposed method which are generated through microwind software. This simulation shows all inputs and output wave and their relations. Here we are giving all input variable wave form.



This shows V/I graph of proposed method. This graph is generated by using V/I simulation of microwind software. Through this graph we are calculating average output current.



Parametric analysis table of propose stack

For the solution of this problem we can used a technique that is called Stack technique. Through this we can improve the Switching speed or response of design circuitry. This technique is also used to reduce leakage current that can improve static power also. Through this table we can give the value of rise time, fall time and output current. This table also shows that the stack technique improves the output current.

Parametric analysis table of propose stack method	
Parameter	Output current (mA)
Value	0.559

Result Analysis

After implementing certain methods, we have found that stack method has proven to be enhancing current, decreasing rise time and fall time, Further it has found that delay is also reduced compared to other techniques.

Comparative Result Analysis

As we have compared different techniques of decreasing elements malfunctioning circuits like noise, charge leakage, charge sharing & delay. The comparison is shown in table 5.2. The comparison has clearly proved that proposed logic has proven advanced than other ones.

Comparative Parametric analysis table

In this table we are giving rise time, fall time and output current values for all previous approaches and proposed stack technique. Through this table we compare all values output current and says whose technique is best all of them.

Cell	Output current (mA)
Source volt with NMOS	0.497
Source volt with PMOS	0.424
Feedback Keeper	0.0025
Pre-charging internal node	0.47
Proposed stack logic	0.559

Conclusion

Through this technique we can improve rise time, fall time, and output current.

Future Scope

In this method we can improve the rise time, fall time and output current but here we can also increase the power dissipation that is the disadvantage of this method. So in future we can develop a new method that can overcome this problem. In other field work Noise is detected using 90nm technology and determining the various parametric estimations techniques for reducing power dissipation could be employed. The performance of the proposed Noise testing circuits should be improved, technique of improving power dissipation should be employed. With all the effects and errors cause due to scaling should be consider in the design of noise testing circuits ,design and optimization of systems using them.

- The performances of the proposed Noise testing circuits should evaluate in terms of speed, area, and power and other stuck at faults.
- With all non-ideal effects and soft errors cause due to scaling should be consider in the design of Noise testing circuits design and optimization of systems using them.
- The responses from the tested devices were shown to correspond with simulation at lower clock frequency, below at higher clock frequency device is slower in the deep Noise region than it is in the deterministic region. Higher frequency MOSFET models require analysis of parasitic switching capacitances.

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