A Low Power Fine-Grained CG and RTPG Integration Based on DDFF

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Abstract

The technology and speed are always move forward, from low scale integration to large, and very large scale integration**.** The system requirements are also rising up with the continuous advancing process of technology and speed of integration. With the progress of CMOS technology, there is a steady growth in clock frequency and chip capacity. To integrate more functions into each chip require more power. As a result, the power dissipation of digital CMOS design has increased tremendously. So, low power techniques are highly appreciated in current VLSI design. So, the two most widely used techniques to reduce dynamic power and leakage power, clock gating (CG) and power gating (PG), respectively, are expected to be integrated together effectively. Here the OBSC technique is used. In order to extent the application of PG, active mode power reduction method can be used, i.e. RTPG. The proposed work uses a new dual dynamic node hybrid flip-flop (DDFF) instead of conventional FFs. The DDFF offers an area, power, and speed efficiency compared to the conventional flip-flops to incorporate complex logic functions into the flip-flop. As a result, the energy efficient DDFF based active fine-grained CG and RTPG integration can significantly reduce about 20% of power consumption.

Keywords

Clock gating, RTPG, OBSC and DDFF.

1. Introduction

CMOS VLSI Technology is the technology for the fabrication of integrated circuits. Nowadays, it is widely used in many digital circuits because of its less static power consumption, high noise immunity and high integration capacity. Technology and speed are always moving forward, from low scale integration to large, and very large scale integration. The system requirements are also rising up with this continuous advancing process technology and speed of operation. So, in order to continue to improve the performance of circuits and to integrate more functions into each chip, accordingly, more power is required. As a result, the power consumption in CMOS VLSI circuits increases tremendously. Power dissipation in excess is due to dynamic and leakage power with the leakage power having further classification as standby leakage and active leakage.

Dynamic power consumption occurs when the circuit has input toggle (operation mode). Leakage power dissipation occurs when the circuit doesn't operate (Sleep mode) is referred to as standby leakage. On the other hand, leakage power consumed in operation mode is the active leakage. So, the two most widely used techniques to reduce dynamic power and leakage power-clock gating (CG) and power gating (PG),respectively, are expected to be integrated together effectively. Normally, the implementation of CG leads to some redundant operations, which provides the opportunity to apply PG. The large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flop. The proposed work uses a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF. The DDFF offers less area, power, and speed efficiency

compared to the conventional flip-flops to incorporate complex logic functions into the flip-flop. The Integration of CG and PG based on DDFF provides less power along with better speed of performance and it is capable of incorporating complex function into FFs.. Some following Points are:

- **Clock Gating**: Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. An activity driven optimized bus specific clock gating (OBSC) maximizes dynamic power reduction. It chooses only a subset of flip-flops (FF) to be gated selectively, and hence the problem of gated FF selection is reduced from exponential complexity into linear.

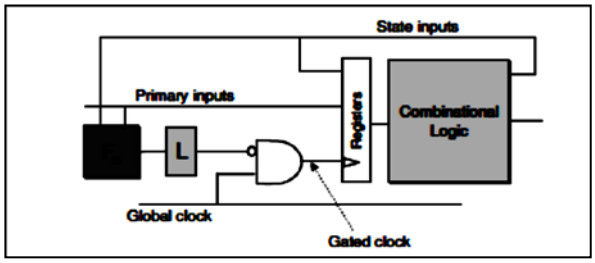

Fig.1. conceptual CG architecture

- **Power gating**: Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to block of the circuits that are not in use. In order to distinguish from traditional Power gating, the power gating that minimizes active leakage power in the operation mode is referred to as Run Time Power Gating(RTPG).

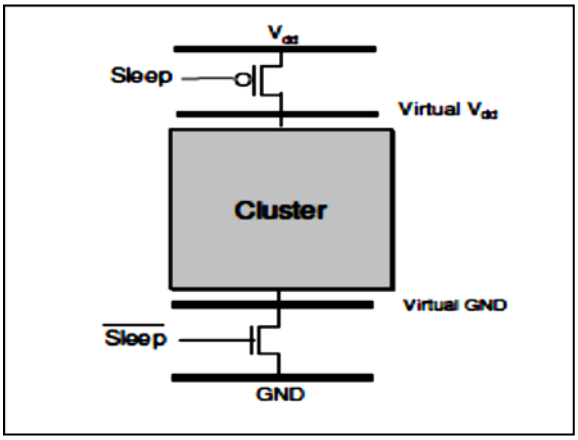

Fig.2. Conceptual PG Architecture

2. System Model

Optimized Bus Specific Clock Gating is very effective technique to maximize dynamic power reduction as shown in fig.3. It chooses only a subset of flip-flops (FF) to be gated selectively, and the problem of gated FF selection is reduced from exponential complexity into linear. It works by comparing the inputs and outputs and gates the clock when they are equal. Considering N FFs in the non-CG circuit, each FF can be chosen as gated or non-gated. Hence, 2N CG solutions are possible and the exponential complexity problem is reduced into linear. Assume that all the FFs are chosen to be gated initially, then the problem is in determining which FFs should be excluded from gating. Heuristically, the FF with the maximum output data toggle rate should be excluded from gating first. This is because that maximum output data toggle rate indicates that minimum clock toggles will be gated, thus power will reduce least or even increase if the FF is gated. More formally, the FF with the maximum output toggle rate is excluded from gating first, then the FF with the second largest output toggle rate is excluded and so on until all the FFs are excluded (i.e., the original non CG circuit).

To extent the application of PG to active mode leakage reduction. The enable signals of gated clock design are 0 exploited to control power switches for combinational logic gates**.** When clock enable 0 ,the power switch is turned off and active mode leakage is cut off. The holder keep the input voltage of non-power gated circuits.

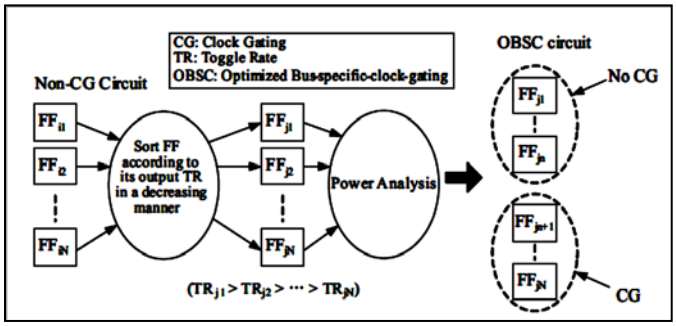

Fig.3. OBSC Technique

3. Previous Work

Integration of CG and RTPG using conventional flip-flops :

A fine-grained CG and RTPG integration in sequential circuits can achieve significant power reduction. An activity driven fine-grained OBSC technique is evaluated that selects only a subset of FFs to gate. Moreover, the clock enable signal generated in the OBSC circuit can be used as the sleep signal in RTPG.

- The conventional flip-flops have power dissipation.
- In some flip-flops like CDMFF, increase in power dissipation due to additional transistors.
- Large pre-charge capacitance
- Redundant power dissipation that results, when the data does not switch for more than one clock (CLK) cycles.

4. Proposed Methodology

A large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flop-flops. An activity-driven fine-grained CG and RTPG integration using energy efficient Dual Dynamic Node Pulsed Hybrid Flip-Flop(DDFF) is proposed to overcome the existing drawbacks. DDFF eliminates the redundant power dissipation

DDFF presents an less area, power, and speed efficient method to incorporate complex logic functions into the flip-flop.

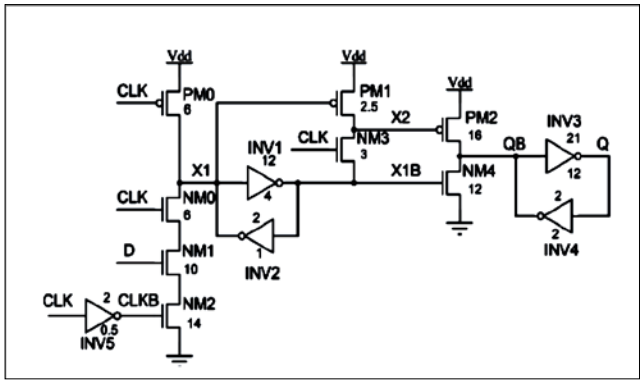

Fig.4. DDFF

In Dual Dynamic Node Hybrid Flip-Flop (DDFF), there are two nodes in the circuit among which one is purely dynamic and another is pseudo-dynamic. So, called as dual dynamic as it is having dynamic frond end and static output, it is hybrid in nature. So this is the reason for calling this flip-flop as DDFF. The clocking is less in DDFF, compared to conventional flip-flops. When input is 0,then only pull-up network is switching, when it is 1,then pull-down network. So, no more power consumption is required, here.

5. Simulation/Experimental Results

The proposed method of combining OBSC and RTPG using DDFF has been tested on 130nm technology. The input datas are generated randomly for 1000 clock cycles, and the simulation result is stored using Tanner simulation environment. Here, the Binary to excess-3 converter has been implemented by using the CG and RTPG integration with DDFF. The power and delay analysis has been done at Tanner simulation environment. Low cost SPARTAN family of FPGA is supported.

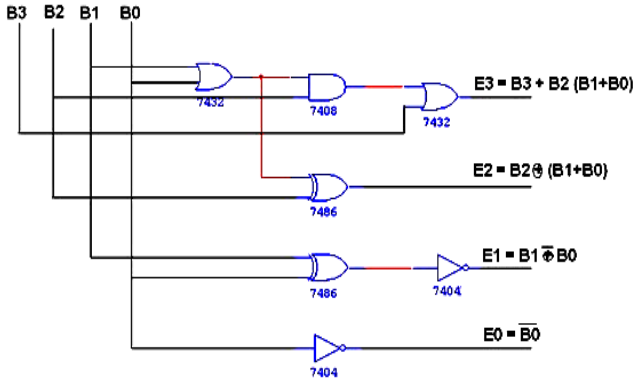

Fig.5.Binary to excess-3 converter circuit

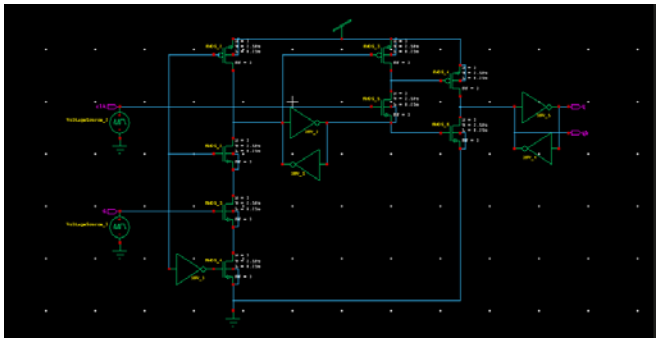

Fig.6. DDFF Schematic in TANNER

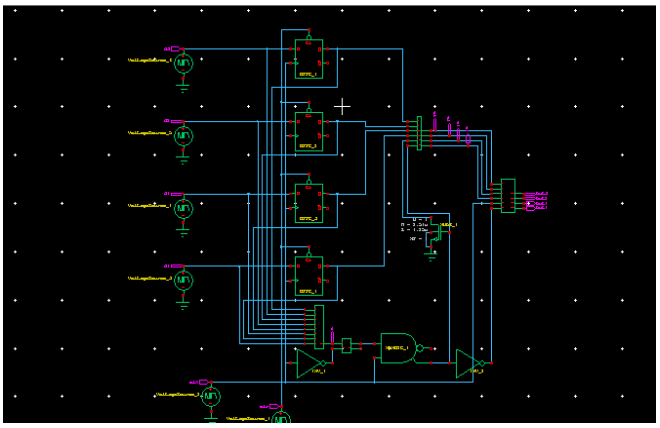

Fig.7.Binary to excess-3 converter using CG and RTPG integration using DDFF.

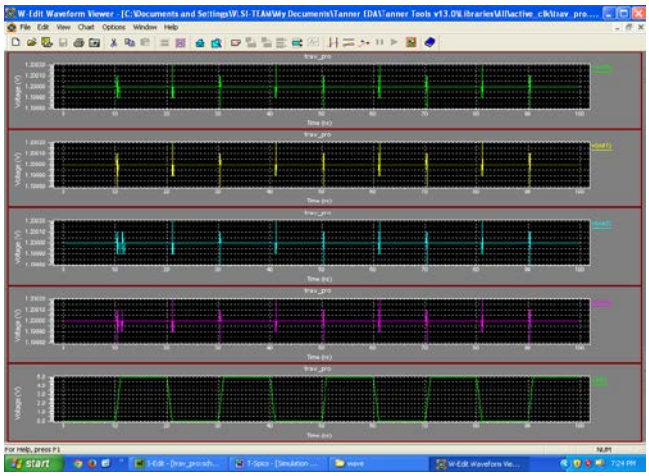

Fig.8. Simulated Wave Form

Table-1: Comparison of power consumption between existing and proposed technique in circuit

	Power Consumption	Delay
CG and PG Integration with conventional flip-flops	45%	1.6ns
CG and RTPG Integration using DDFF	27%	1,1ns

6. Conclusion

As the continuous advancement of CMOS VLSI technology, the power consumption has been increased tremendously. Power consumption represents one of the most important concern in modern systems due to steady growth in number of clock frequency and chip capacity.So,in order to reduce the overall power consumption ,we propose an energy efficient DDFF based CG and RTPG Integrated circuits in modern technology. This method can exhibit lower power dissipation along with comparable speed of performance. Integrating CG and RTPG means to adopt the conditions for clock gating and to power-gate the circuit so that, both the dynamic power and leakage power can be reduced. This active fine-grained power reduction method provides about 20% reduction.

7. Future Scopes

To further reduce the power ,any voltage scaling method can be used.

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