Power Analysis of Sleep and Dream Modes of Multimode Architecture

Archana M C[1], Remya Ramachandran[2]
[1]PG Scholar, [2]Assistant Professor

Abstract

Power consumption is one of biggest challenges in VLSI design. In the past, power has mainly been a concern for chips used in battery-powered devices. During long periods of inactivity, multi-threshold CMOS is very effective for reducing leakage power. There are many techniques to reduce static power. However, they are very much sensitive to process variations which affect manufacturability. Reducing leakage power remains to be one of the key design goals in the mean time. So, a new multi-mode power switch architecture with SPST adder as logic core is proposed. It offers greater power reduction and delay degradation and also requires less design effort. It also assures low leakage power and high tolerance to process variations. To achieve further static power reduction benefits, it can be combined with the existing techniques. The total estimated power consumption of sleep and dream modes are 83mW and 60mW respectively. Hence it is clear that the total power consumption can be decreased to a great extend using intermediate power off modes.

Keywords

Multi-threshold CMOS (MTCMOS), Threshold Voltage (V_t), Leakage Current (IL), Spurious Power Suppression Technique (SPST), Most Significant Part (MSP), Least Significant Part (LSP)

1. Introduction

According to Moore's law, as chip density increases, power consumption is becoming a major problem for the contemporary systems [1]. There are two types of power: static and dynamic. Dynamic power can be reduced by the reduction of supply voltage level, since it is proportional to the square of supply voltage. But the execution time is adversely affected by this reduction. So, transistor threshold voltage is reduced, to maintain system performance. When threshold voltage is decreased, sub-threshold leakage current increases exponentially. So, for technologies below 90 nm, static power is so high that it is comparable in magnitude to dynamic power consumption.

2. System Model

A structure with intermediate power-off mode, which reduces the time required for recovering from idle mode at the expense of reduced leakage current suppression, is proposed. Similar structures were proposed by different authors. They extended this tradeoff between wake-up overhead and leakage power savings into multiple power-off modes. Hence the circuit is put into an intermediate power-off mode (i.e., low-power state), instead of consuming power by remaining in the active mode during the short periods of inactivity, which is determined by the length of the idle period and the wake-up time. The higher are the power savings achieved when the period of inactivity is longer.

3. Previous Work

There are many techniques evolved for reducing leakage power. MTCMOS technology is effective for reducing the same. It is a variation of CMOS chip technology which has transistors with multiple threshold voltage to reduce delay

and power. An approach is to use dual V_t libraries [3]. It suppresses leakage current, but reduces the performance.

Use of high V_t power switches between the circuit and power supply or ground rail can be used to decrease power [2], [3], [5]. During idle mode, these switches are turned off, there by suppressing leakage current. Its drawback is the large current rush during core reactivation and wakeup time. This limitation of power switches can be overcome by using intermediate power of modes. Wakeup time is the time required for recovering from idle mode. So, the circuit is put into a low power state or appropriate power of mode, instead of consuming power by remaining in the active mode [4]. Higher power savings can be achieved when the period of inactivity is longer, by using most aggressive power-off modes.

The previous architectures have several drawbacks. First, it cannot be easily extended to support more than two intermediate power-off modes and thus it cannot be used for high-performance circuits since the power reduction potential cannot be fully exploited. Next, a significant amount of power is consumed by the architecture and this reduces the advantages offered by the power switches. They are also very sensitive to process variations, which can affect its manufacturability and predictability adversely. Also, as it consists of analog components, it is not easily testable.

In this paper, we present an effective and robust multimode power-gating architecture that has none of the above drawbacks of the previous architectures. The proposed structure requires minimal design effort since it is very simple. It is considerably smaller and offers greater power savings for similar wake-up times.

4. Proposed Methodology

Standby power reduction is important in implementing low power systems. Static power becomes more prominent with device scaling.

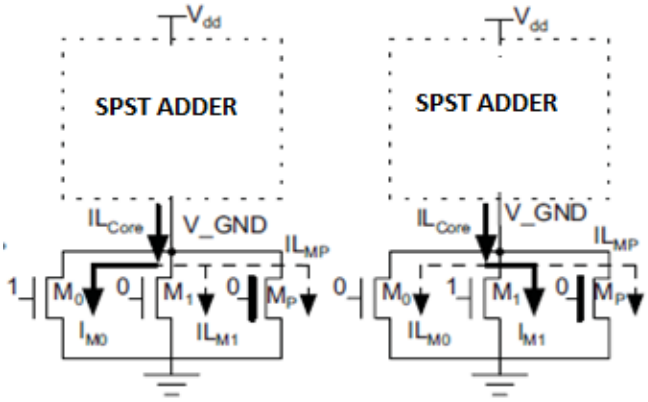

Fig.1: Multimode architecture: (a) dream mode (b) sleep mode.

Fig.1 presents the multimode power switch architecture. It consists of three transistors M_P, M_0 and M_1. M_P is the main power switch transistor with high threshold voltage and remains on only during active mode. Transistors M_0 and M_1 are low threshold voltage transistors and corresponds to intermediate power of modes i.e., dream and sleep modes respectively. They are turned on only during the corresponding power of modes.

1) Active Mode: All transistors are on.
2) Snore Mode: All transistors are off. The leakage current of core is equal to total leakage current flowing though each transistor, which is very small..
3) Dream Mode: M_0 is on and others are off as in Fig 1(a).Since M_0 is on, the current flowing through it increases.($I_{MO} > I_{LMO}$) and hence the total current increases. The exact value of I_{MO} depends on M_0 transistor's size. The voltage level at $V_{\_GND}$ is now lower than V_{dd} ($V_{\_GND} < V_{dd}$).Compared to snore mode, static power is higher, but less wakeup time.
4) Sleep Mode: M_P, M_0 are off and M_1 is on, as in Fig 1(b).When M_1 is on, the total current again increases. Thus, voltage at V_{GND} node is further reduced compared to dream mode and thus wakeup time decreases.

The core part is implemented using SPST (Spurious Power Suppression Technique) adder which reduces power dissipation of combinational VLSI designs. It separates the design into two parts: most significant part(MSP) and least significant part(LSP). The main advantage of using SPST adder

is that it turns off the MSP when it does not affect the computation results to save power.

Fig.2 shows an SPST adder. Between the eighth and ninth bits, the 16 bit adder is divided into MSP and LSP [2]. The input data of MSP remain unchanged when MSP is necessary. But it becomes zeros when MSP is negligible. This is to avoid glitching power consumption. The effective data range of arithmetic units is detected by the detection logic. The data controlling circuits of SPST latch a portion of data when it does not affect the computation results to avoid useless data transition occurring inside the arithmetic units. This data controlling unit brings evident power reduction.

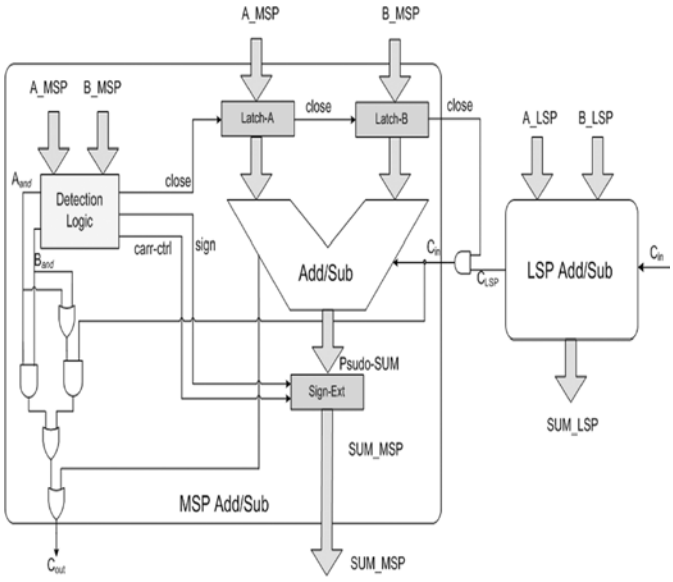

Fig.2: SPST adder

The detection logic unit decides whether to turn off MSP or not. The two operands of MSP enter the detection logic unit and based on some Boolean equations, this unit determine whether the input data of MSP should be latched or not.

SPST adder will avoid the unwanted addition and thus minimize power dissipation. Eliminating the spurious computations will not only save the power consumed inside the SPST adder but also reduce the glitching noises.

5. Simulation/Experimental Results

The multi-mode power switch architecture is synthesized in Spartan 2E starter board as the evaluation development board. The family is Spartan 2E, the device used is XC2S600E, the package is FG676 and the speed is -7. The top level source type is HDL, the synthesis tool is XST (VHDL/Verilog), and the simulator is ISE Simulator (VHDL/Verilog). The power analysis is done using XPower. The power analysis of sleep and dream modes are obtained as follows:

Table-1: Actual parameter values of sleep mode

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.8		
Dynamic		27.72	49.90
Quiescent		15.00	27.00
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Power			83.50
Startup Current		500. 00	

The actual parameter values of sleep mode are given above. The voltage is shown in V, the current in mA and the power in mW. The startup current is 500 mA and the Vccint is 1.8V.The total power is 83.50mW.

Table-2: HTML Power Report of sleep mode

Power summary	I (mA)	P (mW)
Total estimated power consumption		83
Vccint 1.80V:	43	77
Vcco33 3.30V:	2	7
Inputs:	22	39
Logic:	4	7
Outputs:		
Vcco33	0	0
Signals:	2	4
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

The HTML Power Report of sleep mode is shown in Table 2. The current is given in mA and the power in mW. The current from the inputs is 22mA and the power is 39mW. The Vccint is 1.8V and the total estimated power consumption is 83 mW.

Table-3: Actual parameter values of dream mode

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.8		
Dynamic		14.94	26.89
Quiescent		15.00	27.00
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Power			60.49
Startup Current		500. 00	

The actual parameter values of dream mode are given above. The voltage is shown in V, the current in mA and the power in mW. The startup current is 500 mA and the Vccint is 1.8V.The total power is 60.49mW.

Table-4: HTML Power Report of dream mode

Power summary	I (mA)	P (mW)
Total estimated power consumption		60
Vccint 1.80V:	30	54
Vcco33 3.30V:	2	7
Inputs:	14	26
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	1	1
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

The HTML Power Report of dream mode is shown in Table 4. The current is given in mA and the power in mW. The current from the inputs is 14mA and the power is 26mW. The Vccint is 1.8V and the total estimated power consumption is 60mW.

6. Conclusion

In this work, a new power-gating scheme that provides multiple power-off modes is designed. The design offers the advantage of simplicity and required minimum design effort. It is very much tolerant to process variations and is scalable to more than two power off modes. The design requires significantly less area and consumes much less power than the previous design. The multi-mode power switch architecture is synthesized in Spartan 2E starter board. The power analysis is done using XPower. The power analyses of various modes i.e. sleep and dream modes are obtained. From the power analysis it can be viewed that the power consumption of sleep mode is 83mW. The total estimated power consumption of dream mode is 60mW. Hence it is clear that the total power consumption can be decreased to a great extend using intermediate power off modes.

7. Future Scopes

As future work, the designing of the SPST adder with gate replacement technique can be done. The major advantage of gate replacement is that it does not require gate structure modification and is also compatible with standard cell based design flow. Thus power consumption can again be reduced to a great extend.

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Author's Profile

Archana M C has received her Bachelor of Technology degree in Electronics and Communication Engineering from Malabar College of Engineering and Technology in the year 2013. At present she is pursuing M.Tech in VLSI Design at Nehru College of Engineering and Research Centre, Thrissur. Her areas of interest include Signal Processing, Image Processing, Communication and VLSI.

Remya Ramachandran has received her B.Tech Degree in Electronics and Communication Engineering in the year 2008 from Calicut University, Kerala and M.E. Degree in Applied Electronics from Hindusthan College of Engineering and Technology, Coimbatore. At present she is working as an Assistant Professor in the Department of Electronics and Communication Engineering at Nehru College of Engineering and Research Centre, Thrissur. Her areas of interest are Image Processing, Communication, Signal Processing and VLSI.