Optimization, Analysis and Comparison of two stage and three stage Operational Amplifiers using 0.3µm process technology for SCMOS

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Abstract - This paper discuss physical design optimization methodologies and frequency analysis of two stage and three stage ie. Multistage CMOS operational amplifiers and analyze the effect of various parameters on the characteristics of Operational amplifiers using submicron CMOS Spice models specifically 300nm C5 process CMOS technology. In the paper Quiescent point and response curves are plotted for AC and DC characteristics of 4 different topologies of 2 stage operational amplifiers and a single 3 stage operational amplifier are tabulated for suitable frequency ranges. Transients are also plotted from nanoseconds scale to microseconds scale. Subsequently FFTs are also proposed at frequency range from 1 MHz to 25 GHz. By results and reasons in this paper two stage and three stage topologies are suitable choices for low voltage and high performance applications.

Keywords - Operational Amplifiers, CMOS , Quiscent Point analysis, Operating Point, AC and DC analysis

1. INTRODUCTION

Operational Amplifiers are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modelling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuitsare becoming increasingly more difficult to improve upon. The classic Widlar op amp architecture, originally developed for bipolar devices[10], has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower trans conductance of CMOS devices as well as the gain reduction due to short channel effects that

come into play for submicron CMOS processes.

2.AMPLIFIERS

Operational amplifiers typically are composed of either two or three stages consisting of a differential amplifier, a gain stage and an output stage as seen in Figure 1. In some applications, the gain stage and the output stage are one and the same if the load is purely capacitive. However, if the output is to drive a resistive load or a large resistive load, then a high current gain buffer amplifier is used at the output. Each stage plays an important role in the performance of the amplifier.

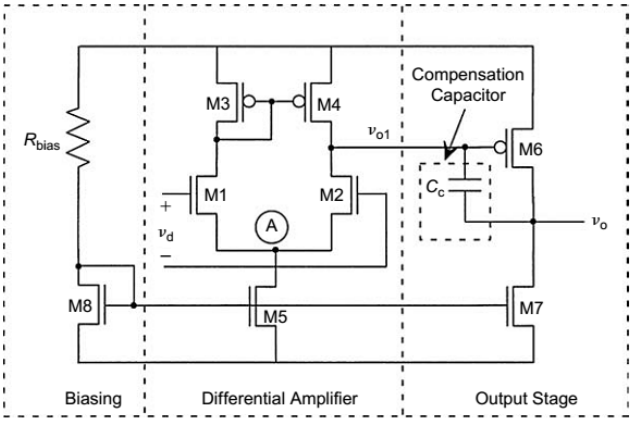


Fig.1 Basic two stage operational amplifier

The differential amplifier offers a variety of advantages and is always used as the input to the overall amplifier. Since it provides common-mode rejection, it eliminates noise common on both inputs, while at the same time amplifying any differences between the inputs. The limit for which this common mode rejection occurs is called common-mode range and signifies the upper and lower common mode signal values for which the devices in the diff-amp are saturated. The differential amplifier also provides gain. The gain stage is typically a common-source or cascade type amplifier. So that the amplifier is stable, a compensation network is used to intentionally lower the gain at higher frequencies. The output stage provides high current driving capability for either driving large capacitive or resistive loads.

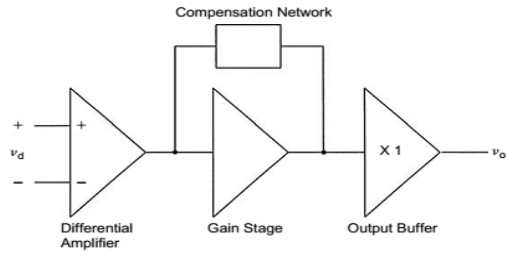


Fig.2. Block Diagram of a generic amplifier

The output stage typically will have low output impedance and high signal swing characteristics. In some cases, it may be advantageous to add bipolar devices to improve the performance of the circuitry. These will be presented as the multi stage opamp circuits are analysed.

3. TWO-STAGE CMOS OPERATIONAL AMPLIFIER

Operational Amplifiers are the backbone for many analog circuit designs. Operational amplifiers are one of the basic and important circuits which have a wide application in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the operational amplifiers. Larger the bandwidth and gain, higher the speed and accuracy of the operational amplifier are a critical element in analog sampled data circuit, such as SC filters, modulators [4]. The first block is a differential amplifier. It has two inputs which are the inverting and non-inverting voltage. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore the block can be excluded. In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage.

As this stage uses differential input unbalanced output differential amplifier, so it provide required extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region.

Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of operational amplifier or improves the slew rate of the operational amplifier. Even the output stage can be dropped: many integrated applications do not need low output impedance; moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the operational amplifier is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used the circuit, it is an operational transconductance amplifier, OTA. The purpose of the compensation circuit is lower the gain at high frequencies and to maintain stability whennegative feedback is applied to operational amplifier[7].

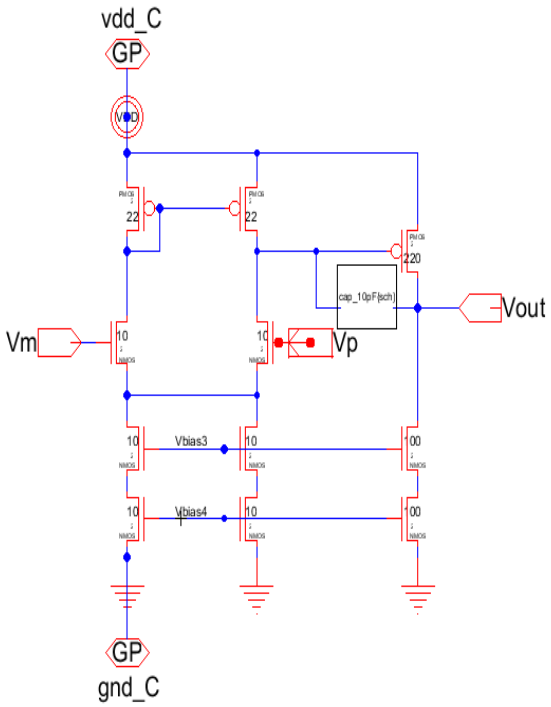


Fig. 3 Schematic for topology 1 for two stage operational amplifier

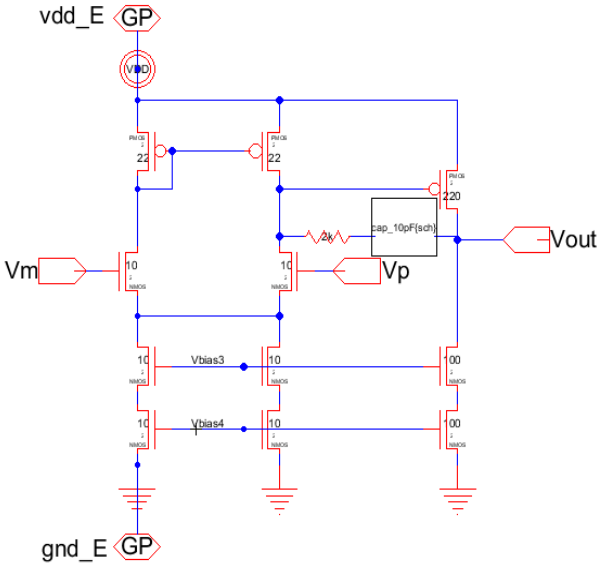


Fig. 4 Schematic for topology 2, 2 stage operational amplifier

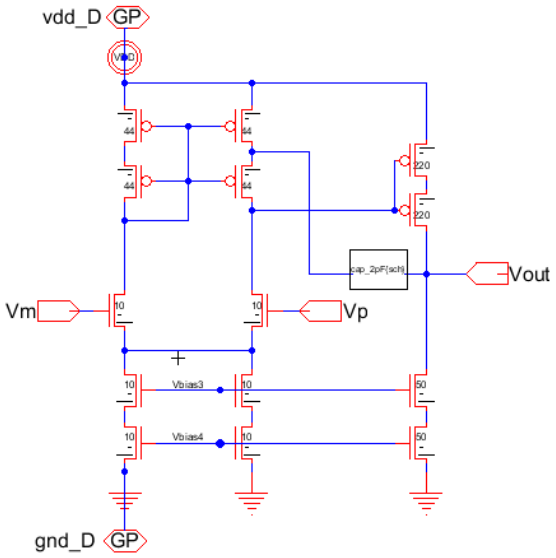


Fig. 5 Schematic for topology 3, two stage operational amplifier

4. THREE-STAGE CMOS OPERATIONAL AMPLEFIER

Three stage operational amplifiers are used in applications where low power is required or that can operate with low supply voltage or with minimal power from VDD. In comparison to two –stage operational amplifiers the bias circuit is to be developed can pull more current from VDD than the operational amplifiers it biases. So I have used two circuit architectures for biasing circuits. For proper operation of the output stage floating current sources are generally preferred.

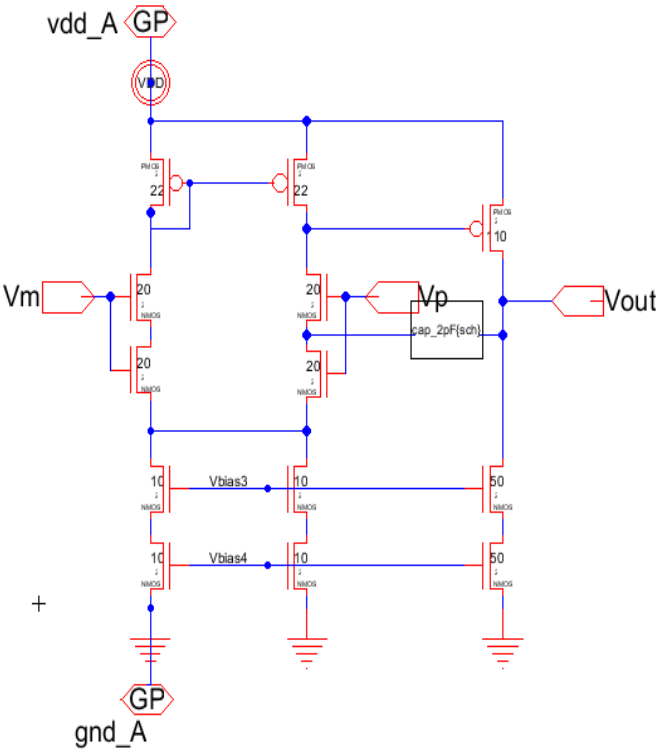


Fig.6 Schematic for topology 4, two stage operational amplifier

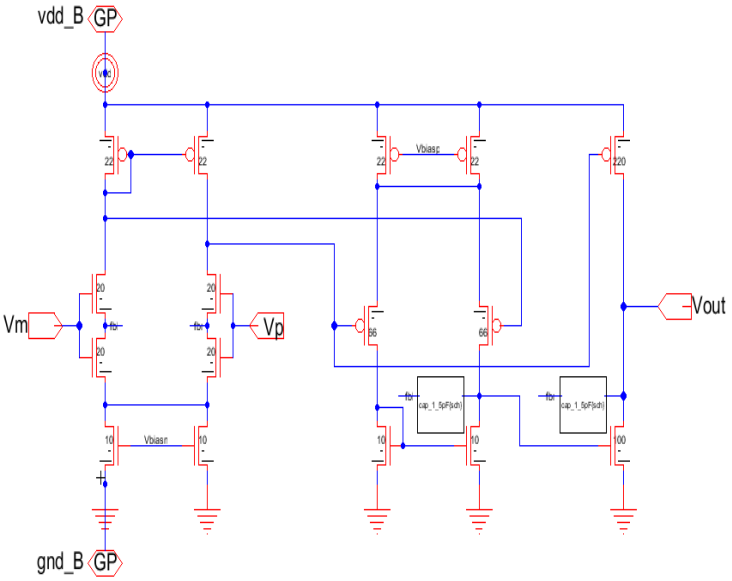


Fig.7 Schematic for topology 3, two stage operational amplifier

Towards keeping a large gain and lowering the power supply voltage, considering the three stage operational amplifier above. The design is cascade of two different differential amplifier stages followed by a common source amplifier. If we connect a resistive load to the output of the common source stage, the overall operational amplifier gain remains relatively high due to the cascaded gain of two differential amplifier stages. This topology of operational amplifier i.e. more than two stages is a sort of compensation. The compensation of capacitors within the operational amplifier for overall improvement in the desired operational amplifier characteristics[3,6].

5. DESIGN METHODOLOGY AND DESIGN FLOW

It is assumed that all transistors are in saturation for the above relationships. The design in this project is a two-stage op amp with an n-channel input pair. The op amp uses a dual-polarity power supply (Vdd and Vss) so the ac signals can swing above and below ground and also be centered at ground.[38] Design flow approach regarding the same is as follows

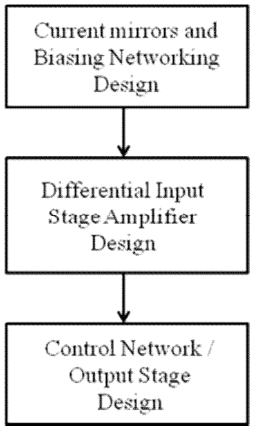


Fig.8. Design Flow used for OpAmp Design

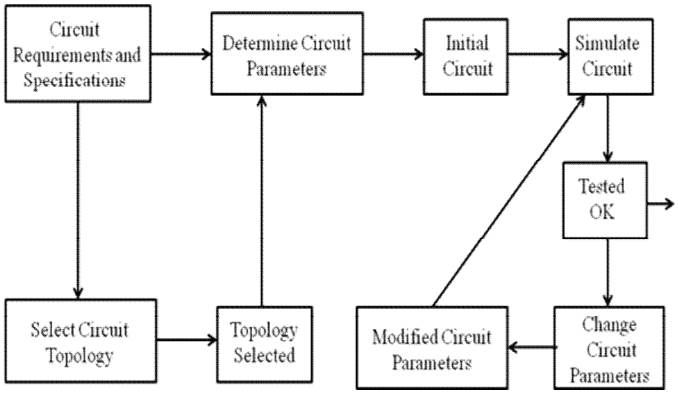


Fig.9. Design Procedure

6. SIMULATION/EXPERIMENTAL RESULTS

*** SPICE deck for cell Opamp_2Stage_1_Sim_Op{sch} from library opamp

--- Operating Point ---

V(net@1):	2.49236	voltage
V(vout):	2.49236	voltage
V(vp):	2.5	voltage
V(vdd):	5	voltage
V(vbiasp):	3.72128	voltage
I(Ccap@1):	-7.47707e-023	device_current
I(Ccap@0):	2.49236e-017	device_current
I(Rbias):	3.72128e-005	device_current
I(Rres@0):	2.49086e-017	device_current
I(Vcm):	0	device_current
I(Vdd):	-0.00132113	device_current
Ix(opamp_2s@0:GND):	-0.00108721	subckt_current
Ix(opamp_2s@0:VBIASP):	-3.72128e-005	subckt_current
Ix(opamp_2s@0:VDD):	0.00108721	subckt_current
Ix(opamp_2s@0:VM):	0	subckt_current
Ix(opamp_2s@0:VOUT):	3.1225e-017	subckt_current
Ix(opamp_2s@0:VP):	0	subckt_current

Fig.10 snapshot for operating point analysis of 2 Stage op-amp Topology-1

*** SPICE deck for cell Opamp_2Stage_2_Sim_Op{sch} from library opamp

--- Operating Point ---

V(net@1):	2.49236	voltage
V(vout):	2.49236	voltage
V(vp):	2.5	voltage
V(vdd):	5	voltage
V(vbiasp):	3.72128	voltage
I(Ccap@1):	-7.47707e-023	device_current
I(Ccap@0):	2.49236e-017	device_current
I(Rbias):	3.72128e-005	device_current
I(Rres@0):	2.49314e-017	device_current
I(Vcm):	0	device_current
I(Vdd):	-0.00132113	device_current
Ix(opamp_2s@0:GND):	-0.00108721	subckt_current
Ix(opamp_2s@0:VBIASP):	-3.72128e-005	subckt_current
Ix(opamp_2s@0:VDD):	0.00108721	subckt_current
Ix(opamp_2s@0:VM):	0	subckt_current
Ix(opamp_2s@0:VOUT):	2.29851e-017	subckt_current
Ix(opamp_2s@0:VP):	0	subckt_current

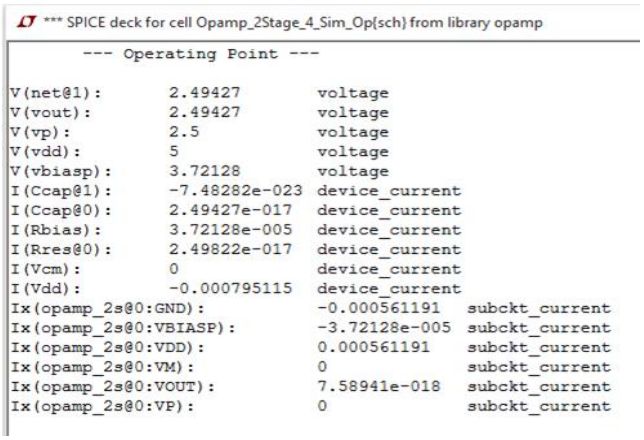
Fig.11 snapshot for operating point analysis of 2 Stage op-amp Topology-2

*** SPICE deck for cell Opamp_2Stage_3_Sim_Op{sch} from library opamp

--- Operating Point ---

V(net@1):	2.49427	voltage
V(vout):	2.49427	voltage
V(vp):	2.5	voltage
V(vdd):	5	voltage
V(vbiasp):	3.72128	voltage
I(Ccap@1):	-7.48282e-023	device_current
I(Ccap@0):	2.49427e-017	device_current
I(Rbias):	3.72128e-005	device_current
I(Rres@0):	2.49822e-017	device_current
I(Vcm):	0	device_current
I(Vdd):	-0.000795115	device_current
Ix(opamp_2s@0:GND):	-0.000561191	subckt_current
Ix(opamp_2s@0:VBIASP):	-3.72128e-005	subckt_current
Ix(opamp_2s@0:VDD):	0.000561191	subckt_current
Ix(opamp_2s@0:VM):	0	subckt_current
Ix(opamp_2s@0:VOUT):	7.58941e-018	subckt_current
Ix(opamp_2s@0:VP):	0	subckt_current

Fig.12 snapshot for operating point analysis of 2 Stage op-amp Topology-3

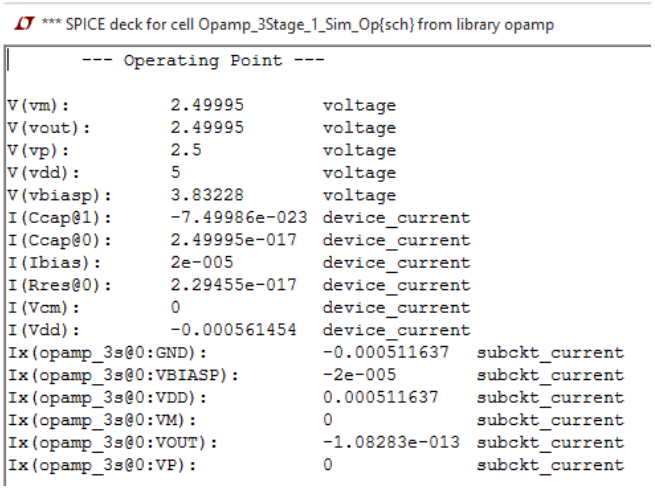


*** SPICE deck for cell Opamp_2Stage_4_Sim_Op{sch} from library opamp

--- Operating Point ---

V(net@1):	2.49427	voltage
V(vout):	2.49427	voltage
V(vp):	2.5	voltage
V(vdd):	5	voltage
V(vbiasp):	3.72128	voltage
I(Ccap@1):	-7.48282e-023	device_current
I(Ccap@0):	2.49427e-017	device_current
I(Rbias):	3.72128e-005	device_current
I(Rres@0):	2.49822e-017	device_current
I(Vcm):	0	device_current
I(Vdd):	-0.000795115	device_current
Ix(opamp_2s@0:GND):	-0.000561191	subckt_current
Ix(opamp_2s@0:VBIASP):	-3.72128e-005	subckt_current
Ix(opamp_2s@0:VDD):	0.000561191	subckt_current
Ix(opamp_2s@0:VM):	0	subckt_current
Ix(opamp_2s@0:VOUT):	7.58941e-018	subckt_current
Ix(opamp_2s@0:VP):	0	subckt_current

Fig.13 snapshot for operating point analysis of 2 Stage op-amp Topology-4



*** SPICE deck for cell Opamp_3Stage_1_Sim_Op{sch} from library opamp

--- Operating Point ---

V(vm):	2.49995	voltage
V(vout):	2.49995	voltage
V(vp):	2.5	voltage
V(vdd):	5	voltage
V(vbiasp):	3.83228	voltage
I(Ccap@1):	-7.49986e-023	device_current
I(Ccap@0):	2.49995e-017	device_current
I(Ibias):	2e-005	device_current
I(Rres@0):	2.29455e-017	device_current
I(Vcm):	0	device_current
I(Vdd):	-0.000561454	device_current
Ix(opamp_3s@0:GND):	-0.000511637	subckt_current
Ix(opamp_3s@0:VBIASP):	-2e-005	subckt_current
Ix(opamp_3s@0:VDD):	0.000511637	subckt_current
Ix(opamp_3s@0:VM):	0	subckt_current
Ix(opamp_3s@0:VOUT):	-1.08283e-013	subckt_current
Ix(opamp_3s@0:VP):	0	subckt_current

Fig.14 snapshot for operating point analysis of 3 Stage op-amp

Table 1 : Quiescent Point Analysis Results for different topologies of Operational Amplifiers

Parameters	2 Stage Topology 1	2 Stage Topology 2	2 Stage Topology 3	2 Stage Topology 4	3 Stage Topology
V(Vout)	2.49236	2.49236	2.49427	2.49427	***2.49995***
V(Vp)	2.5	2.5	2.5	2.5	***2.5***
V(Vdd)	5	5	5	5	***5***
Vbiasp	3.72128	3.72128	3.72128	3.72128	***3.83228***
I(Vdd)	0.00132	0.00132	0.000795	0.000795	***0.000561***
I(Vout)	3.122e-17	2.298e-17	7.584e-18	7.589e-18	***1.0828e-13***

7. CONCLUSION

Keeping in view different applications the Op-amp has been designed. For this first a selection is made for the active device used. Four different topologies of 2 stage operational amplifiers are analyzed for various transients and FFT responses are proposed for calculations for frequencies ranging from 1MHz to 25 MHz Quiescent point analysis is also done for all the mentioned topologies. The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to redesign the circuit for various set of specifications. The responses are simulated using LTSpice and Electric VLSI CAD design tool. The simulated results of the Op-amp are in compliance with the theoretical values.

8. FUTURE SCOPE

3 stage operational amplifier is designed using 0.3 SCMOS process technology. A single topology is compared with 4 different 2 stage Opamp topologies.Operating point analysis is carried out for each. AC analysis is also to be carried out for frequency range 100MHz – 100 GHz. Transient Analysis is also to be carried to suitable time scale preferably 5µs. A FFT analysis is also to be done (using CAD) to verify the high performance operational Amplifier.

REFERENCES

[1] Dr. Soni Changlani, Ayoush Johari “Implementation , analysis and comparison of 2 stage and 3 stage and multistage Operational Amplifiers” CICN IEEE Conference November 2014

[2] Perenzoni, Matteo, Luca Parmesan, and David Stoppa. "A robust, power-and area-efficient gm-control for low-noise operational amplifiers." Analog Integrated Circuits and Signal Processing 82.1 (2015): 209-216.

[3] Grassi, Marco, Jean-Michel Redoute, and Anna Richelli. "Increased EMI immunity in CMOS operational amplifiers using an integrated common-mode cancellation circuit." Electromagnetic Compatibility (EMC), 2015 IEEE International Symposium on. IEEE, 2015.

[4] Tepwimonpetkun, Samattachai, Bhirawich Pholpoke, and Woradorn Wattanapanitch. "Graphical analysis and design of multistage operational amplifiers with active feedback Miller compensation." International Journal of Circuit Theory and Applications (2015).

[5] Ohno, Yasuhiko, et al. "Maximum and minimum voltage sample and hold circuits employing operational amplifiers composed of polycrystalline silicon thin-film transistors." Future of Electron Devices, Kansai (IMFEDK), 2014 IEEE International Meeting for. IEEE, 2014.

[6] Vigraham, Baradwaj, Jayanth Kuppambatti, and Peter R. Kinget. "Switched-Mode Operational Amplifiers and Their Application to Continuous-Time Filters in Nanoscale CMOS." Solid-State Circuits, IEEE Journal of 49.12 (2014): 2758-2772.

[7] Irom, Farokh, Shri G. Agarwal, and Mehran Amrbar. "Compendium of Single-Event Latchup and Total Ionizing Dose Test Results of Commercial and Radiation Tolerant Operational Amplifiers." Radiation Effects Data Workshop (REDW), 2014 IEEE. IEEE, 2014.

[8] Eschauzier, Rudy GH, and Johan Huijsing. Frequency compensation techniques for low-power operational amplifiers. Vol. 313. Springer Science & Business Media, 2013.

[9] Ahuja, Bhupendra K. "An improved frequency compensation technique for CMOS operational amplifiers." Solid-State Circuits, IEEE Journal of 18.6: 629-633.

[10] Azmi, Nilofar, and D. Sunil Suresh. "DESIGN OF LOW POWER OPERATIONAL AMPLIFIER USING CMOS TECHNOLOGIES." immunity 2 (2014):

[11] Todani, R. I. S. H. I., and ASHIS KUMAR Mal. "Simulator based device sizing technique for operational amplifiers." WSEAS Trans. Circ. Syst 13.1 (2014): 11-28.

[12] Yamatoya, Yuki, Akira Hiroki, and Hirokazu Oda. "Macromodeling of operational amplifiers for overdrive circuit design." Future of Electron Devices, Kansai (IMFEDK), 2015 IEEE International Meeting for. IEEE, 2015.

[13] Cardoso, Guilherme S., et al. "Reliability Analysis of 0.5 µm CMOS Operational Amplifiers under TID Effects." Journal of Integrated Circuits and Systems 9.1 (2014): 70-79.

[14] Petrov, A. S., K. I. Tapero, and V. N. Ulimov. "Influence of temperature and dose rate on the degradation of BiCMOS operational amplifiers during total ionizing dose testing." Microelectronics Reliability 54.9 (2014): 1745-1748.

[15] Cuong, Nguyen Duy, and Tran Xuan Minh. "Design of analog MRAS controllers using operational amplifiers for motion control systems." Information Science, Electronics and Electrical Engineering (ISEEE), 2014 International Conference on. Vol. 2. IEEE, 2014.

[16] Prokopenko, Nikolay N., et al. "The Advanced Circuitry of the Precision Super Capacitances Based on the Classical and Differential Difference Operational Amplifiers." Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2015 IEEE 18th International Symposium on. IEEE, 2015.

[17] Jothimurugan, R., et al. "Improved realization of canonical Chua's circuit with synthetic inductor using current feedback operational amplifiers." AEU-International Journal of Electronics and Communications 68.5 (2014): 413-421.

[18] Kusuda, Yoshinori. "5.1 A 60V auto-zero and chopper operational amplifier with 800kHz interleaved clocks and input bias-current trimming." Solid-State Circuits Conference-(ISSCC), 2015 IEEE International. IEEE, 2015.

[19] Bakerenkov, A. S., et al. "Radiation Degradation Modeling of Bipolar Operational Amplifier Input Offset Voltage in LTSpice IV." Applied Mechanics and Materials. Vol. 565. 2014.

[20] Huijsing, Johan, Rudy J. van de Plassche, and Willy Sansen, eds. Analog circuit design: operational amplifiers, analog to digital convertors, analog computer aided design. Springer Science & Business Media, 2013.

[21] Sakurai, Satoshi, and Mohammed Ismail. Low-voltage CMOS operational amplifiers: Theory, Design and Implementation. Vol. 290. Springer Science & Business Media, 2012.

[22] Nakhostin, M., et al. "Use of commercial operational amplifiers in a low cost multi-channel preamplifier system." Radiation Physics and Chemistry 85 (2013): 18-22.

[23] Gray, Paul R., and Robert G. Meyer. "MOS operational amplifier design-a tutorial overview." Solid-State Circuits, IEEE Journal of 17.6 (1982): 969-982.

[24] Lipka, B., and U. Kleine. "Design of a cascoded operational amplifier with high gain." Mixed Design of Integrated Circuits and Systems, 2007. MIXDES'07. 14th International Conference on. IEEE, 2007.

[25] Baker, R. Jacob. CMOS: circuit design, layout, and simulation. Vol. 18. Wiley-IEEE Press, 2011.

[26] Rao, K. Radhakrishna, and S. Srinivasan. "A band pass filter using the operational amplifier pole." Solid-State Circuits, IEEE Journal of 8.3 (1973): 245-246.

[27] Aggarwal, S., and A. B. Bhattacharyya. "Low-frequency gain-enhanced CMOS operational amplifier." IEE Proceedings G (Circuits, Devices and Systems)138.2 (1991): 170-174.

[28] Aininzadeh, H., Mohammad Danaie, and Reza Lotfi. "A low-power design methodology for single-stage operational amplifiers." Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. International Conference on. IEEE, 2006.

[29] Peng, Mingsheng, et al. "A 1-V quasi rail-to-rail operational amplifier with a single input differential pair." Region 5 Technical Conference, 2007 IEEE. IEEE, 2007.

[30] Schlogl, F., Horst Dietrich, and Horst Zimmermann. "High-gain high-speed operational amplifier in digital 120nm CMOS." SOC Conference, 2004. Proceedings. IEEE International. IEEE, 2004.

[31] Klinke, R., B. J. Hosticka, and H. Pfleiderer. "A very-high-slew-rate CMOS operational amplifier." Solid-State Circuits, IEEE Journal of 24.3 (1989): 744-746.

[32] Karanicolas, Andrew N., et al. "A high-frequency fully differential BiCMOS operational amplifier." Solid-State Circuits, IEEE Journal of 26.3 (1991): 203-208.

[33] Lipka, B., and U. Kleine. "Design of a cascoded operational amplifier with high gain." Mixed Design of Integrated Circuits and Systems, 2007. MIXDES'07. 14th International Conference on. IEEE, 2007.

[34] Holman, W. Timothy, and J. Alvin Connelly. "A compact low noise operational amplifier for a 1.2 µm digital CMOS technology." Solid-State Circuits, IEEE Journal of 30.6 (1995): 710-714.

[35] Gulati, Kush, and Hae-Seung Lee. "A high-swing CMOS telescopic operational amplifier." Solid-State Circuits, IEEE Journal of 33.12 (1998): 2010-2019.

[36] Duque-Carrillo, J. Francisco, et al. "1-V rail-to-rail operational amplifiers in standard CMOS technology." Solid-State Circuits, IEEE Journal of 35.1 (2000): 33-44.

[37] Chaudhari, Haresh S., Nilesh D. Patel, and Jaydip H. Chaudhari. "Optimization and Simulation of Two Stage Operational Amplifier Using 180nm and 250nm Technology."
[38] Chaudhari, Haresh S., and Nilesh D. Patel. "Simulation Of Two Stage Operational Amplifier Using 250nm And 350nm Technology." International Journal of Engineering 2.4 (2013).
[39] Randal E. Bryant, Kwang - TingCheng , Andrew B Kahang, Kurt Kreutzer, Wojciech Maly,Richard Newton, Lawerance Pileggi, Jan M Rabaey, Alberto Saniovanni-Vincentelli, "Limitations and Challenges of CAD Technology for CMOS VLSI"
[40] Boise state university online tutorials at http://cmosedu.com/cmos1/electric/electric.htm.
[41] VLSI Open Source CAD Tools http://www.vlsiacademy.org/open-source-cad-tools.html
[42] Electric Static Free Software. July 2004 http://www.staticfreesoft.com

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