

Application of Feed forward-Regulated Cascode OTA for the design of 10 Gigahertz M-ary Modulator Circuits

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Abstract - This paper demonstrates 10 gigahertz M-ary ASK circuit design using a Feed forward-regulated cascode OTA. The feed forward-regulated cascode OTA can operate up to 10 GHz bandwidth with a large transconductance of 100 mS. The feed forward-regulated cascode OTA is used to design various high frequency analog circuits like inductor less oscillator however the OTA is not used to design the digital communication techniques. This paper emphasizes in the design of high speed data rate and high carrier frequency up to 10 GHz modulation scheme. The output for Quaternary ASK results up to 10 GHz carrier frequency. The work is mathematically analyzed and the simulated results shows the accuracy of the designed system. The results are discretely shown for 10 GHz and 5 GHz carrier frequency. Mentor graphics is used for the simulation and layout of the designs.

Keywords - Feed forward, OTA, Quaternary Amplitude Shift Keying.

1. INTRODUCTION

There are hardly few OTAs (Operational Transconductance Amplifiers) which operates in gigahertz range. The feed forward-regulated cascode OTA proves to be an excellent operational transconductance amplifier to break the gigahertz range with high transconductance. There are several important microwave applications that are well-suited for implementation with high-speed OTAs, such as phase shifters [1] and oscillators [2], [5]. The communication domain being rapidly increasing and the use of very high frequency in gigahertz range, this paper demonstrates the design analysis of digital modulation schemes using the feed forward-regulated cascode OTA. In contrast to OTAs using feedback-regulated cascode topologies, the feed forward approach can diminish time delay in the cascode regulation and thereby significantly increase its operating speed. The feed forward OTA can operate within a bandwidth of 10 GHz with extremely high transconductance compared to other OTAs [3]. A reliable high-speed data communication has been a major concern over a limited channel bandwidth, in the harsh wireless environments [1]. The high demand of

low cost, low volume, wireless communication systems, has put pressure on integrating as many parts as possible in a single chip. Also, the need for long duration of operating with a single low-voltage supply in system demands low-power and low-voltage designs [2]. Current-mode devices show advantages over their voltage-mode counterparts including increased bandwidth, higher dynamic range, better suitability for operation in reduced supply environments, simpler circuitry, lower power consumption etc. The feed-forward OTA being a current mode device proves to be excellent in high frequency circuits. The organization of this paper is as follows: A short discussion on feed forward-regulated cascode OTA is discussed in sec-4. The design methodology of Quaternary ASK is discussed in sec-5. The comparative analysis and simulation results are discussed in sec-6, and the paper is concluded in sec-7.

2. SYSTEM MODEL

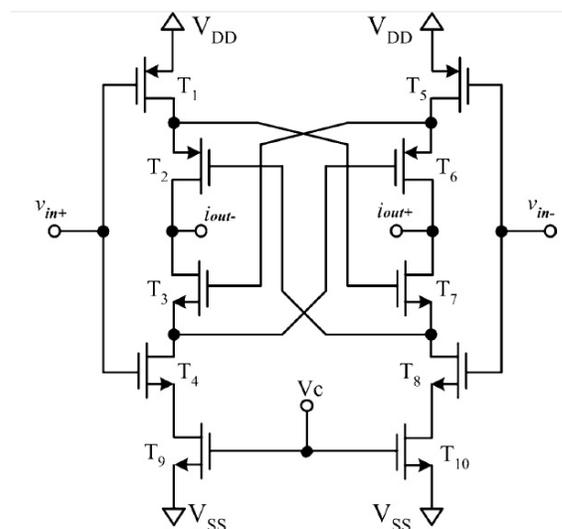


Fig. 1 CMOS fully differential OTA using negative feed forward-regulated cascodes. [3]

In this paper, the design of various digital modulation schemes, Quaternary ASK, QFSK and QAM using feed

forward-regulated cascode OTA is shown. The application of feed forward OTA in the field of communication is described in this paper, ensuring the communication schemes working in the range of 5 GHz to 10 GHz carrier frequency with high data rate. The operation of communication schemes in the range of 10 GHz is a vital beneficial for our modern communication system. The mathematical formulations are shown in this paper. Mentor graphics is used for the simulation and layout process. The simulation results are distinctly shown for carrier frequencies up to 10 GHz for Binary ASK, and 5 GHz for Quaternary Amplitude shift keying.

3. PREVIOUS WORK

A basic digital modulation scheme using OTA has been proposed in [1] and [2], however it fails to design the circuits to work in the range of 5-10 GHz. The digital modulation schemes designed using OTAs had low data rate and the OTAs used for the design had low transconductance. All the demerits of the previous design has been eliminated by the use of feed forward-regulated cascode OTA.

4. FEED FORWARD-REGULATED CASCODE OTA

The feed forward-regulated cascode OTA in fig. 1 has differential inputs and differential outputs, which allows the circuit to be used in both positive and negative feedback system configurations [3]. The OTA contains two pMOS regulated cascodes (T_1/T_2 and T_5/T_6) and two nMOS regulated cascodes (T_3/T_4 and T_7/T_8) where the pMOS cascodes have the same configuration as the nMOS cascodes and their DC currents are controlled by the two DC current sources at the bottom (T_9 and T_{10}) [3]. Instead of local negative feedback, this OTA uses a negative feed forward method for its four regulated-cascodes to speed up the regulating process. They are realized by two pairs of cross connections between the pMOS cascodes and the nMOS cascodes, which also work as the coupling between the two differential paths [3]. In the proposed OTA, the feed forward topology can completely remove the regulating delay and it also eliminates the need for any DC block and additional biasing circuitry when this OTA is cascaded with copies of itself, which greatly simplifies overall system design.

Here for our design purpose we have replaced the transistor T_9 and T_{10} and instead of supplying a controlling voltage we have supplied a controlling current. The current output is only taken from i_{out+} , hence only one output terminal is required. There by reduces the number of transistors and also the transconductance will now be proportional to controlling

current I_C . The overall block diagram of the feed forward OTA will be as shown in fig. II.

The relationship between the output current and differential input voltage is given as

$$I_{out} = gm(V_{in}) \quad (1)$$

Where gm is the trans conductance of the OTA,

$V_{in} = V_1 - V_2$, is the differential input voltage

V_1 is the input to the non inverting terminal and V_2 is the input to the inverting terminal.

$$gm = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right) I_c} \quad (2)$$

μ_n is the mobility of the carrier,

C_{ox} is the capacitance of MOS.

$\frac{W}{L}$ is the width by length ratio of MOS.

I_c is the controlling current.

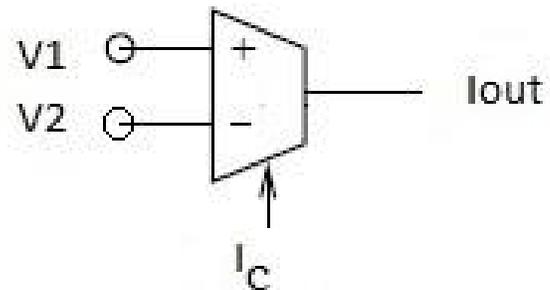


Fig. 2 Block diagram of OTA

Here, the transconductance can be easily tuned using the controlling current I_C . The range for the controlling current is from $-200\mu A$ to $500\mu A$. This predefined feed forward OTA is used for the design of digital communication schemes which is discussed in the section below.

5. DESIGN METHODOLOGY OF QUATERNARY ASK

The design of M-ary ASK is proceeded first with the design of n-bit to 2^n voltage level converter, which is used as digital

to analog converter. The n bit of data is then converted to 2ⁿ voltage levels which is multiplied using an OTA based multiplier that operates up to 10 GHz. The output of the multiplier gives M-ary ASK modulated output with carrier frequency of 10 GHz.

5.1 LEVEL CONVERTER

The n-bit of data is first converted to 2ⁿ voltage levels through a level converter, conventionally digital to analog converter. Fig. 1 represents the design of n-bit to 2ⁿ level converter using OTA. The design is already discussed by the author in [1] paper. However in this paper, the design uses a feed-forward cascade regulated OTA, which has improved the data rate to an exceptional level.

Fig 3. represents n-bit to 2ⁿ voltage level converter, where the output v₀ gives 2ⁿ distinct voltage levels. Equation (3) represents the mathematical equation for n bit to 2ⁿ level converter.

$$V_0 = \frac{\left\{ \frac{B_0}{R_1} + B_1 gm_1 + \frac{B_2}{R_3} + B_3 gm_3 + \dots + \frac{B_{n-1}}{R_{n-1}} + B_{n-1} gm_{n-1} \right\} R'}{\left\{ 1 + \left(\sum_{i=1}^{n-1} \frac{1}{R_i} + \sum_{i=1}^{n-1} gm_i \right) R' \right\}} \tag{3}$$

Where gm_i represents the transconductance of ith OTA.

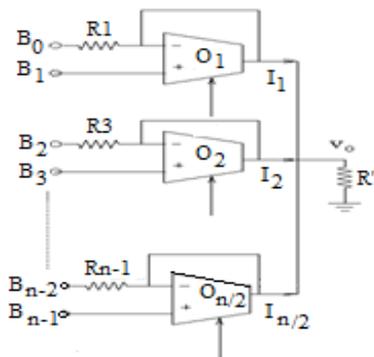


Fig. 3 n bit to 2ⁿ level converter.[1]

With the use of feed-forward cascade OTA, the following advantages are achieved to the previous work.

- a) the data rate has increased.
- b) the step size between each voltage level has increased as the transconductance of feed forward cascade OTA is very high up to 100ms.

- c) low rate of the device has also increased because of less delay time.

5.2 ASK MODULATOR

The output of the level converter is then processed through an OTA based multiplier, where the 10 GHz carrier frequency is applied in one of the input terminal.

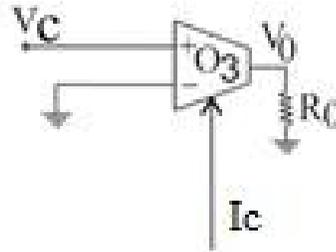


Fig. 4 OTA based multiplier

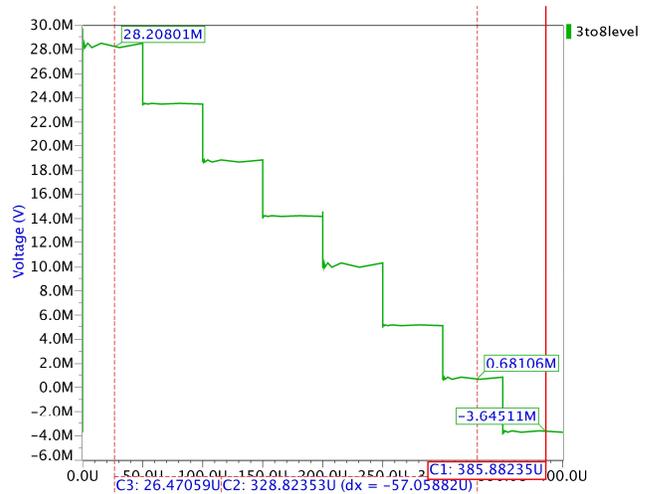


Fig. 6 3 to 8 level converter

Fig. 4 represents an OTA based multiplier, where V_C is the carrier signal of 10GHz. The other input to the multiplier is from the controlling current I_C. Here the controlling current is directly proportional to the transconductance gm, and the controlling current will be the output current of the n-bit to 2ⁿ level converter.

$$V_0 = V_C \cdot gm \tag{4}$$

Where V_C is the carrier signal, and gm is the transconductance driven by the n-bit to 2ⁿ level converter.

The output of the multiplier gives the M-ary ASK modulated waveforms, modulated in the carrier wave of 10GHz.

6. SIMULATION/EXPERIMENTAL RESULTS

The basic concept of design methodology was already described by the author in previous work, however in this paper, the slight change in the design methodology shows a drastic change in the output.

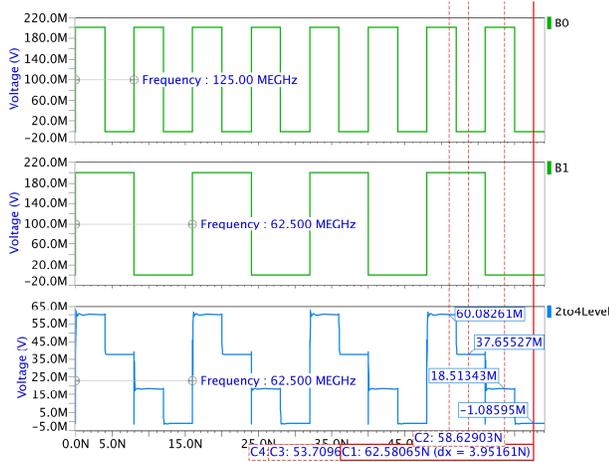


Fig. 5 2 to 4 level converter

Table 1 Comparison between previous and present work

Previous work	Present work
a) General OTA was used for the design	a) Feed forward Cascode regulated OTA
b) Carrier frequency 2 GHz	b) Carrier frequency 10 GHz
c) Transconductance 10u	c) Transconductance 100m
d) Low step size for DAC	d) Very high step size for DAC

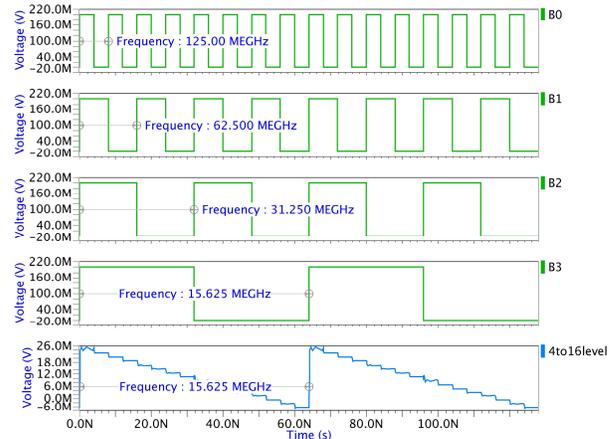


Fig. 7 4 to 16 level converter

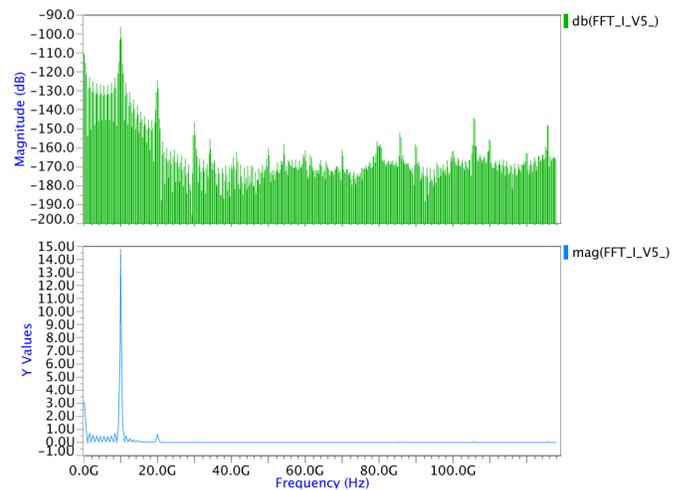


Fig. 8 FFT of 10 GHz ASK modulated signal

6. CONCLUSION

The application of feed forward regulated cascade OTA in communication system has proved to be of immense advantageous. The carrier frequency has increased from 2 GHz to 10 GHz, and the data rate of the system has also increased. The increase in transconductance of the OTA has improvised the step size of level converter (DAC), which proves to be advantageous when designing more than 4-ary modulation schemes. The advantages of using feed-forward OTA in communication schemes is that the OTA blocks can be further cascaded to increase the design upto 8-ary modulators, and the carrier frequency can range upto 10 GHz

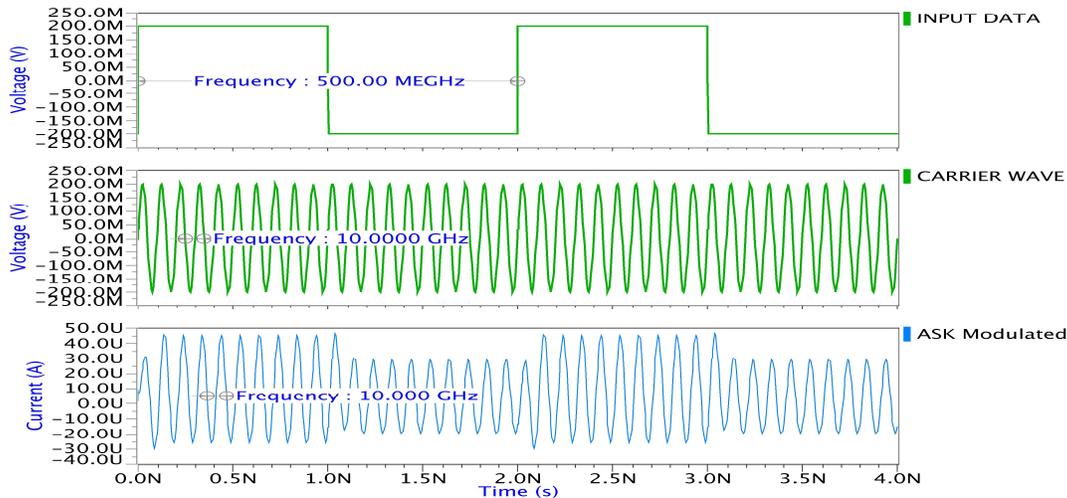


Fig. 9 ASK modulated waveform at 10GHz

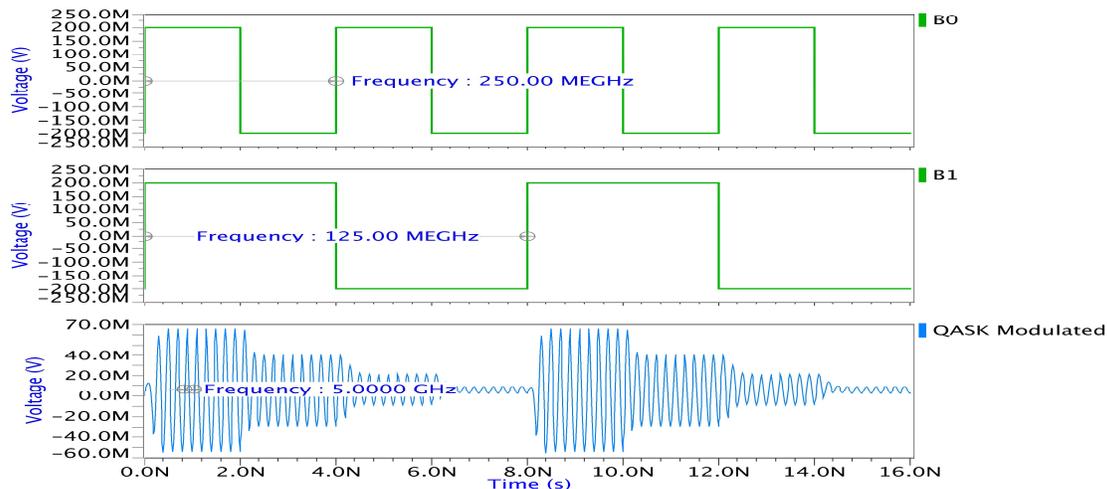


Fig. 10 QASK modulated waveform at 5 GHz

7. FUTURE SCOPES

The work is further carried out for the design of M-ary FSK and QAM. The oscillator producing 10 GHz of frequency is already designed and now it shall be used for the design of M-ary FSK. The Communication schemes shall be benefited with the design as it shall be operated in low power and high frequency.

REFERENCES

- [1] Das, Ratan, Surya Prakash Tamang, Mousumi Bhanja, Koushik Ghosh, and Bonnie Ray. "A new design technique of OTA based M-ary modulator and demodulator." In *Microelectronics and Electronics (PrimeAsia), 2013 IEEE Asia Pacific Conference on Postgraduate Research in*, pp. 268-272. IEEE, 2013.
- [2] Bhanja, Mousumi, Surya Prakash Tamang, Ritika Das, and Baidyanath Ray. "Design Methodology of High Frequency M-ary ASK, FSK and QAM." *Journal of Circuits, Systems and Computers* 24, no. 10 (2015): 1550152.
- [3] Zheng, You, and Carlos E. Saavedra. "Feedforward-regulated cascode OTA for gigahertz applications." *Circuits and Systems I: Regular Papers, IEEE Transactions on* 55, no. 11 (2008): 3373-3382.
- [4] Wang, Zhenhua. "Current-mode CMOS integrated circuits for analog computation and signal processing: a tutorial." *Analog Integrated Circuits and Signal Processing* 1, no. 4 (1991): 287-295.
- [5] Roy, Arabinda, Sekhar Mandal, Baidya Nath Ray, and Prasanta Ghosh. "Synthesis of CMOS OTA based communication circuit." In *Electrical and Computer*

Engineering, 2008. ICECE 2008. International Conference on,
pp. 107-112. IEEE, 2008.

- [6] Sanchez-Sinencio, Edgar, and Jose Silva-Martinez. "CMOS transconductance amplifiers, architectures and active filters: a tutorial." In *Circuits, Devices and Systems, IEE Proceedings-*, vol. 147, no. 1, pp. 3-12. IET, 2000.
- [7] Lewinski, Artur, and Jose Silva-Martinez. "OTA linearity enhancement technique for high frequency applications with IM3 below-65 dB." *Circuits and Systems II: Express Briefs, IEEE Transactions on* 51, no. 10 (2004): 542-548.
- [8] Grasso, Alfio Dario, Gaetano Palumbo, and Salvatore Pennisi. "Three-stage CMOS OTA for large capacitive loads with efficient frequency compensation scheme." *Circuits and Systems II: Express Briefs, IEEE Transactions on* 53, no. 10 (2006): 1044-1048.
- [9] Murmann, Boris. "A/D converter trends: Power dissipation, Scaling and digitally assisted architectures." In *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp. 105-112. IEEE, 2008.

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