# A Review on Design and Implementation of Digital PLL for Clock Generation

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***Abstract - The digital phase-locked loop, DPLL, is a circuit that is used frequently in modern integrated circuit design. Consider the waveform and block diagram of a communication system, Digital data1 is loaded into the shift register at the transmitting end. The data is shifted out sequentially to the transmitter output driver. At the receiving end, where the data may be analog (and, thus, without well-defined amplitudes) after passing through the communication channel, the receiver amplifies and changes the data back into digital logic levels. The next logical step i n this sequence is to shift the data back into a shift register at the receiver and process the received data. However, the absence of a clock signal makes this difficult. The DPLL performs the function of generating a clock signal, which is locked or synchronized with the incoming signal. The generated clock signal of the receiver clocks the shift register and thus recovers the data. This application of a DPLL is often termed a clock-recovery circuit or bit synchronization circuit. This paper basically reviews the design and implementation of DLL.***

***Keywords- DPLL, Clock generator, VCO, SoC, Charge pumps, PFD, Oscillator.***

## 1. INTRODUCTION

Digital Phase locked loop is a mixed signal analog integrated circuit. Digital PLL is the heart of many communication as well as electronic systems. Mostly a higher lock PLL range with lesser locking time and should have tolerable phase noise. The most versatile application of a digital PLL is for clock generation or synchronization, clock recovery, communication systems and frequency synthesizers. In high performance digital systems like processors digital PLL or DPLL are commonly used to generate well timed on chip clock signals. Modern RF circuits or wireless mobile communication systems use PLL for synchronization , timing based synthesis, skew and jitter reduction. Digital PLL is extensively used in advanced communication systems, electronic and medical instrumentation systems. The PLLs are an integrated part of larger circuits on a single chip.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

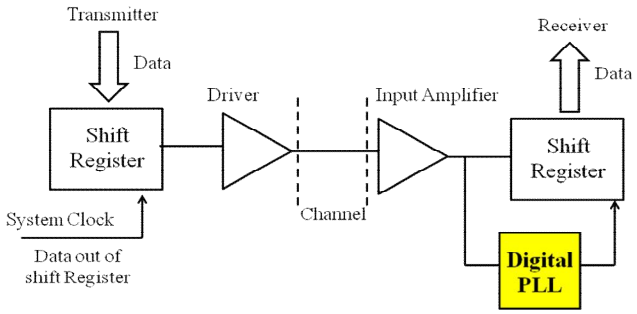


Figure.1. Block Diagram of a communication system using DPLL

Strong interest in the implementation and design of digital PLLs (DPLL) started because of the popularity of large scale integrators (LSIs) [1]. Aside from the obvious advantages associated with digital systems, a digital version of PLL alleviates some of the problems associated with its analog counterpart; namely:

1. Sensitivity to dc drift and component saturation.

2. Difficulty in building higher order loops.

3. Need for initial calibration. [4]

## I. CLASSIFICATION OF PLL

There are many types of design which were proposed earlier. The broad classification of PLL Design is presented in Table 1. Any PLL is designed by modifying one of three stages phase detector, loop filter, voltage controlled oscillator.

A PLL is a device which locks an output signal phase relative to an input reference signal phase. PLL's are typically divided into broad categories listed.

In addition, with the ability to perform sophisticated signal processing on the IC chips, DPLL's are more flexible and versatile than analog PLL's [1]. The DPLL is still a semi analog circuit and is referred to as hybrid PLL. The all digital PLL (ADPLL) and software PLL has recently gained

increased attention. The ADPLL is built entirely from logic circuits and has replaced the classical DPLL in many applications, especially digital communications [1].

**Table 1**

**Classification of PLL Categories**

| S.No. | PLL | Phase Detector | Loop Filter | Oscillator |
|---|---|---|---|---|
| **1.** | Linear PLL or Analog PLL | Analog | Analog | Voltage Controlled Oscillator (VCO) |
| **2.** | Digital PLL | Digital | Analog | Voltage Controlled Oscillator (VCO) |
| **3.** | Digital PLL | Digital | Digital | Digitally Controlled Oscillator (DCO) |
| **4.** | Software PLL | Software | Software | Software |

## II. DESIGN

PLL: A basic PLL is a negative feedback system that receives an incoming oscillating signal and generates an output waveform that exerts the same phase/frequency relationship as the input signal. This is achieved by constantly comparing the phase of output signal to the input signal with a phase/frequency detector (PFD).

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase hangs that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CKref to produce a high-frequency clock CKout this is known as clock synthesis. A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference

In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

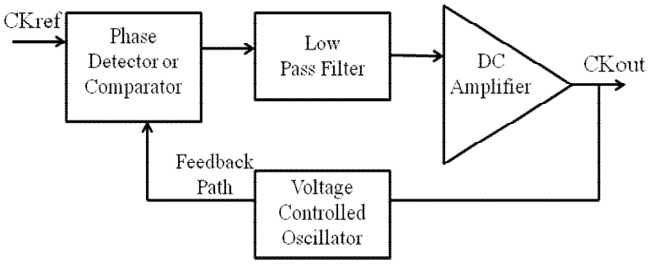


Figure.2. Block Diagram of Digital PLL

The basic operation of PLL can be divided into 3 steps.

1. The phase detector catches the phase difference between two inputs and generates an error signal Vpd whose average value is linearly proportional to the phase difference.
2. A loop filter is then used to suppress the high frequency components of the phase detector output allowing the average value to control VCO frequency.
3. Oscillator generates an output signal whose frequency is a linear function of the control signal out of the loop filter.

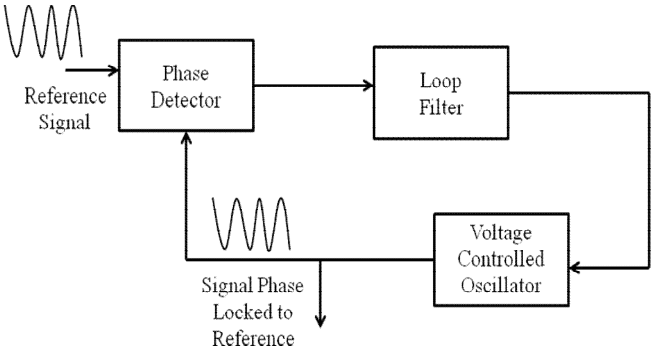


Figure.3 Basic block diagram of PLL(Analog or Digital)

Figure 3 shows the waveform of the reference signal and PLL output when loop is locked.

The generated signal is feedback to the input of the phase detector and another phase comparison is started until the phase difference achieves a fixed relationship [3][5].

## III. DIGITAL PLL DESCRIPTION

A PLL is comprised of a phase/frequency detector (PFD), charge pump (CP), a low-pass filter (LPF), and a voltage-controlled oscillator (VCO). An input reference frequency (FREF) is sent to one of the PFD inputs. The other input terminal of PFD is driven by a divided version of VCO output signal to provide a negative feedback to the loop. The PFD detects differences in phase and frequency between the

reference and feedback inputs to generate compensating up (UP) or down (DN) signals.

If reference input (FREF) occurs before that of feedback input (FBK), indicating that the VCO is running too slowly, the PFD produces a UP signal that lasts until the rising edge of the FBK. If the FBK occurs before FREF, the PFD produces a DN signal that is triggered on the rising edge of the FBK input and lasts until the rising edge of FREF. If the FBK frequency is less than that of FREF, the pulse-width of the UP signal is greater than the width of DN signal and vice versa. In this way, the PFD produces control signals that are unique for any phase and frequency relationship between reference and feedback signal.

These control signals are then passed through CP and a loop filter to generate a control voltage (Vctrl), which feeds into a VCO, the frequency of which is dependent on the control voltage input. Thus, based on phase/frequency relationship of input and feedback signal, the VCO can be forced to run faster or slower, which finally locks to oscillate at a fixed frequency once two inputs at PFD are phase/frequency aligned. The output of the VCO is an internally generated oscillator waveform. At steady state, the PLL system frequency is: The PLL is designed to operate within a limited band of input frequencies. If FREF is outside the defined band, circuit will not lock, thus FVCO will be different than expected one.

FPLL = FVCO = FREF * P

Where:

FPLL = PLL frequency

FREF = Reference frequency

P = Feedback divider

The range of FREF from Fmin to Fmax where the PLL remains in locked condition is called the lock range of the PLL. Out of lock range (i.e., Fmax < Fref < Fmin), the PLL becomes unlocked. When the PLL is unlocked, the VCO oscillates at the frequency Ffr, called the free-running frequency of VCO. The PLL can achieve the lock again if FREF gets close enough to Ffr. This narrow band (∆Fc) of frequency, centered at Ffr so that the initially unlocked PLL acquires the lock again, is called the 'capture range of the DPLL.

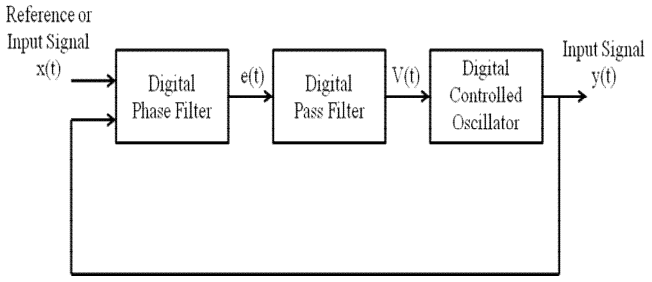


Figure.4 Block diagram of a Simple DLL

PLL has three operating states: - free running, capture and lock. In free running state, the feedback loop is open and there is no

external input frequency, the VCO oscillates at the natural frequency. In the capture state, an external input signal is necessary and feedback loop should be complete. PLL is in process of acquiring frequency lock in capture state. In lock state, the output frequency of VCO is locked onto the frequency of external input signal.

Digital PLL consists of Digital phase detector, analog loop filter, voltage controlled oscillator. Digital phase detector is shown in Figure. 4 where A is input signal tx and B is feedback signal through tx. As shown in Figure. 4, if A=1 then QA=1 and if at the same time B=1, then QB=1. Output of AND gate is connected to RESET pin when both are 1 and vice- versa. The e(t) is (QA– QB) and is used to detect difference between the phase and frequency. Filters are used after charge pump to reduce the ripple as shown in Figure. 5. Charge pump converts phase/frequency detector (PFD) logic states into analog signal suitable for voltage controlled oscillator [7].

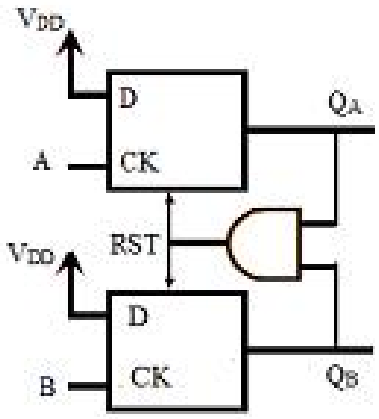


Figure.5 Digital Phase/ Frequency Detector

### IV. Architecture of PLL

The architecture of a charge-pump PLL is shown in Figure 4. A PLL comprises of several components. They are (1) phase

or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider.

*A) Phase frequency Detector*

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". Figurebelow shows a traditional PFD circuit. the phase detector is basically a comparator. It compares the phase of external input

signal to the phase of VCO output signal. The phase comparator produces an error voltage e(t) which is due to difference in phase between two signals as shown in Figure. 2. It is used to determine when VCO and reference signal are aligned [3][6].

If there is a phase difference between the two signals, it will generate "UP" or "DOWN" synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand if the

feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs [6-7] are generally preferred over traditional PFD.

*B) Charge Pump and Loop Filter*

Loop filter [1][3][5][6] is used to remove high frequency of the phase detector output and then applied to the input of VCO. Based on the property of PLL, the loop filter is made using low pass filter (LPF). It has to pass only the DC component and block the AC components.

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value IPDI which should be insensitive to the supply voltage variation [8]. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure below

When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is IPDI with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is IPDI with a negative polarity. The passive low pass loop filter is used to convert back the charge pump current into the voltage. The filter should be as compact as possible [9].The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if Fref rising edge leads Fin rising edge and will decrease if Fin rising edge leads Fref rising edge. If the PLL is in locked state it maintains a constant value.

*C) VCO/DCO IN PLL*

Electrical oscillators are used in all kinds of electronic systems. Oscillators that will be discussed in this paper will find its application in synchronization of control logic with various analog and digital integrated circuits. Oscillatory behavior is ubiquitous in all physical systems specially in memory and mixed signal integrated circuits, in frequency and communication systems. Oscillators are the prime requirements of circuits needing time references and also to synchronize operations. An ideal oscillator would provide perfect time reference i.e. a perfect periodic signal [1], but oscillators are corrupted by undesired noise.

A variety of Oscillators are available but the principle of operation, the frequency of oscillation, their fabrication with respect to different CMOS logics relative, process technologies and their performance in noisy environment is different from one class of oscillators to other.

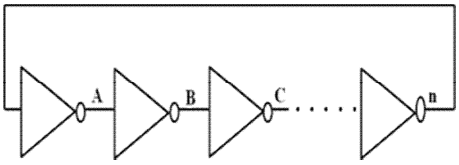


Figure.6. Ring Oscillator realization with n digital inverters

This ring oscillator is designed to be controlled in a oscillation frequency by a voltage input. The physical design of the very same will include C5 process, 300 nm process technology simultaneously various design rule checks and network consistency checks were performed. CMOS inverter ring oscillators offer numerous advantages like tuning ranges, signal swing and a small chip area.

C.1 BARKHAUSEN CRITERIA

The Barkhausen criterion is used to determine the oscillation startup condition. The Barkhausen stability criterion is necessary but not sufficient for oscillation[4].

$$|H(j\omega)| \geq 1 \qquad \text{(i)}$$

$$\angle\, |H(j\omega) = \pi \qquad \text{(ii)}$$

The criteria for oscillation is not well understood, there is no known sufficient criteria for oscillation.

Them the circuit may oscillate at ω if the conditions (i) and (ii) are met called the Barkhausen criterion.

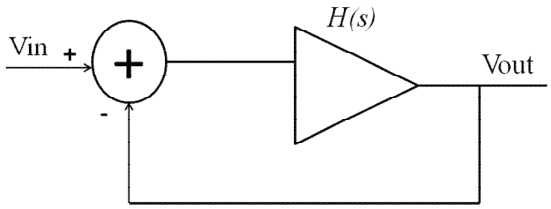


Figure.7 Generalized Feedback System[6]

D) Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the

VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Figure below.

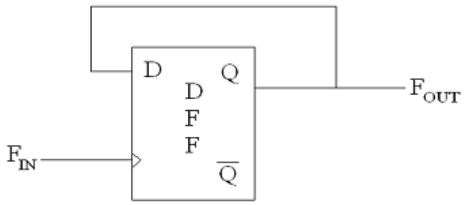


Figure.8 Schematic of a simple DFF based divide by 2 frequency divider circuit

## V. PERFORMANCE COMPARISONS

In this review[1], the proposed novel successive approximation algorithm to improve the frequency and phase locking time of BBPHD-based ADPLL without much scarification of output clock jitter. 790ns locking time demonstrates that such design is suitable for microprocessor, which needs to switch to a different frequency during dynamic frequency scaling. Although achieving fast-locking, it still needs to stall CPU during the locking process because the oscillator is reset and the frequency changes dramatically during SAR search. Therefore, future works will be to design an ADPLL that can both achieve fast locking and a smooth frequency change in DCO.

**TABLE II**

**Performance Comparisons of DPLL Implementations with respect to various process technologies [1]**

| | | | | |
|---|---|---|---|---|
| **CMOS Process Technology** | 180nm | 130nm | 65 nm | 45 nm |
| **Core Area** | 0.14 $mm^2$ | 0.2 $mm^2$ | 0.07$mm^2$ | 0.07$mm^2$ |
| **Power** | 26.7 mW | 16.5 mW | 1.81 mW | 16mW |
| **Output Range** | 62-616 MHz | 0.3-1.4 GHz | 90-527 MHz | 0.8-12 GHz |
| **Locking Time** | NA | 3.5us | NA | 46us |
| **Jitter RMS** | 7.28ps | 3.7ps | 8.64ps | 1.32ps |

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**TABLE III**

**Performance Comparisons of ADPLL[2]**

| | | |
|---|---|---|
| **Process** | 180 nm | 180nm |
| **Power Consumption** | 26.7 mW | 25.02 mW |
| **Resolution** | - | 2.1 ps |
| **Jitter Performance** | 56 ps | 32.86 ps |
| **Frequency Range** | 62 MHz- 616 MHZ | 400 MHz- 860 MHz |

**TABLE IV**

**Comparison of various technologies used in DPLL**

| Technique | Input Frequency | Output Frequency | Power | Area |
|---|---|---|---|---|
| BW Tracking[11] | 28 -225 MHz | 1.80 GHz | - | - |
| Frequency Estimation | 220 KHz- 8 MHz | 28 – 446 MHz | - | 330x250 $\mu m^2$ |

| | | | | |
|---|---|---|---|---|
| Algorithm for fast locking[12] | | | | |
| Delay based technique[13] | 12 MHz | 2.40 GHz | 12 mW | 0.24 $mm^2$ |
| Adaptive loop gain Control (ALGC)[14] | 50 MHz | 0.30-1.40 GHz | 16.50 mW | 0.20$mm^2$ |
| Feed Forward Compensation[15] | 376 MHz | 4 to 416 MHz | 11.39 mW | 2400 $\mu m^2$ |
| Bang Bang Algorithm [16] | 156.25 MHz | 40 GHz | 46 mW | 0.30 $mm^2$ |
| Auto Calibration [17] | 5-44 MHz | 1.90-3.80 GHz | - | 0.65$mm^2$ |
| Digital Calibration [21] | 26 MHz | 1.80 GHz | 41.6 mW | 3.50$mm^2$ |

In review [2], An all-digital PLL was proposed and designed with a tristate inverter delay cell based LPI-TDC using 0.18$\mu$m CMOS process. The proposed delay-cell in LPI-TDC is exploited to obtain high performance and low power consumption. Other parts in the proposed ADPLL such as DLF and DCO are implemented to reduce jitter, and to generate a proper frequency through accurate digitized control words. The proposed ADPLL performs better than the conventional ones, and it will be a good reference for the future work.

## VI. CONCLUSION

In this paper a review for Digital PLL clock generator design and analysis is presented. The PLL circuit consumes a power of 11.9 mW from a 1.8 V D.C. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.

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