A Review: Network-on-Chip Design for Efficient Computation

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Abstract- These days, every electronic system, starting from a mobile phone to large satellite, has a System-on-Chip. SoCs have undergone quick evolution and still progressing at a swift pace. Because of this explosive development of semiconductor industry, the devices are scaling low at a fast rate and thus, the System on Chip today has become communication-centric. NoC is one of the efficient on-chip communication architecture for System on Chip where a large number of computational and storage blocks are integrated on a single chip. Network on Chip have tackled the disadvantage of System on Chip as well as they are scalable. A proficient routing algorithm can enhance the performance of Network on Chip. There are various types of routing algorithms are studied. Some are smart routing algorithm which combines the features of both deterministic and adaptive routing. Some partially adaptive routing methods are analyzing in this review paper.

Keywords- Network-on-Chip (NoC), Multi-Core NoC (MCNoC), System-on-Chip (SoCs).

I. INTRODUCTION

The demand of the human race is gradually increasing day by day. People always prefer a small electronic device having many more features in it. Thus VLSI industry found a new a paradigm i.e. System on Chip (SoC). According to this paradigm different electronic or computing systems are embedded on a single chip. Those computing or electronic systems are also called as intellectual property cores. Routing algorithm is an important design concept of Network on Chip. The function of routing algorithm is to determine an efficient route for the data or packets to transfer from source to destination. The routing algorithms may be classified in various basis i.e. i) Adaptivity nature ii) Fault tolerance nature iii) Number of destinations. The routing algorithm is a crucial task in network layer.

Since the introduction of research into multi-core chips more than a decade ago, on-chip networks have emerged as an important and growing field of research. As core counts increase, there is a corresponding increase in bandwidth demand to facilitate high core utilization and a critical need for scalable interconnection fabrics such as on-chip networks. On-chip networks will be prevalent in computing domains ranging from high-end servers to embedded system-on chip (SoC) devices. This diversity of applications platforms led to research in on-chip networks spanning a variety of disciplines from computer architecture to computer-aided design, VLSI and embedded systems.

Evolution of On chip Networks

The necessity of packet switched on chip networks. Here the discussion will start from various communication infrastructures for a System on Chip and how NoC became so popular in this domain. Here there is some discussion about some common terms in data networks and its relation to the NoC. This discussion will go on with main components and important design concepts of NoC. There are three common communication systems for system on chip point to point communication and shared bus system.

Point to Point Communication

Previously the designers prefer the direct point to point connection for the communication in system on chip. Here the resources or cores are allowed to communicate directly through wires which are connected to each cores.

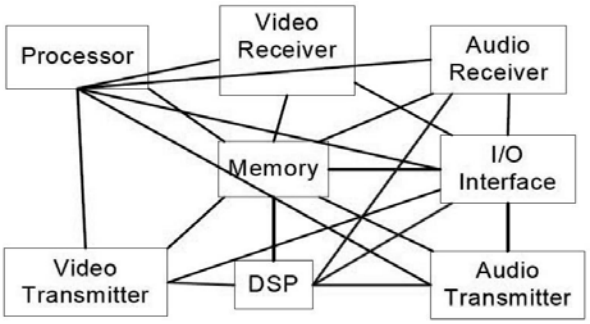

Fig 1.1 Point to point communication system

This system doesn't need any priority providing system or arbitration unit. For a system on chip having more number of cores, this communication system requires large routing area, large routing delay and large number of pins for each core and becomes very complex in wiring point of view. When direct point to point interconnections are used for

communication, in communication system the class of signal and delays occurred for routing can be detected. As a result wiring area and cost is greatly reduced. There are different buses present in literatures such as hierarchical, segmented, pipelined buses etc. So there are many advantages of this communication system. But still it has some disadvantages like due to contention and arbitration data movement becomes slow. In the scalability point of view this system is not a fair choice as it can be scaled upto certain limits otherwise its efficiency will be very bad. A shared bus is shown in Figure 1.2.

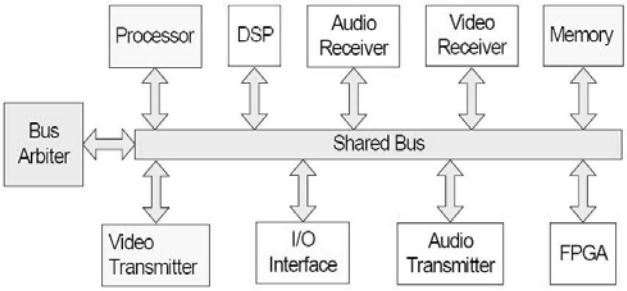

Fig. 1.2 Shared Bus System for SoC

Basic Concepts of NoC

NoC follows the simplified rules or protocols of general data communication network. The discussion is about the relation of NoC to the layered communication of OSI model.

II. SYSTEM ARCHITECTURE

Design Concepts of NoC

The important design concepts of NoC are described which are backbone of NoC. They are

- *Topology*
- *Switching techniques*
- *Routing algorithms*

The performance of NoC depends upon these above concepts. The researchers have been researching in same area from past few years. The design of a NoC in HDL requires a lucid understanding of the different concepts of NoC like topology, routing strategies, switching etc. choosing a topology is paramount in designing a NoC as routing strategy, flow control etc. are based on it. Of the various topologies studied. The Mesh is quite easier to design and it can also easily integrate regular-sized IP cores on a lone chip. The pictorial representation of a 4×4 Mesh is as shown in given *Fig. 2.1*, with two unidirectional channels amongst two routers or a computational resource and a router

Router Architecture

The basic building block of any NoC is its router which is responsible for guiding the data packets to the next router or an IP as per a routing strategy specified inside it [26]. The assumption made in this design is that all the resources are homogeneous and deliver packets of same length.

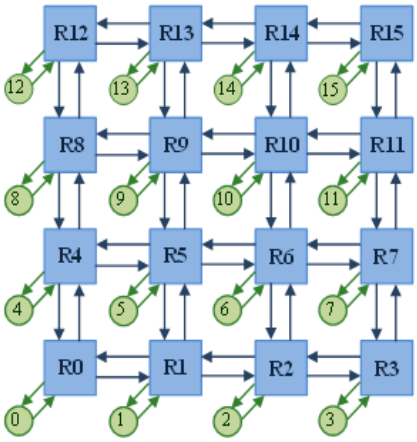

Fig. 2.1 4×4 Mesh Architecture

A better understanding of the functionality of a router can be obtained by looking at the path traversed by a data packet inside the router. Assume a data packet comes into the router through one of the input ports of a FIFO Buffer. Then the FIFO Buffer sends the destination address part of the packet to the Arbiter. The arbiter performs the arbitration process and on request grant, sends the arbitration consequence to the Crossbar block. It also sends a *grant* signal to the FIFO. The FIFO then pops the data packet leading to its injection into the input port of crossbar. The packet then traverses through the crossbar from its input port to corresponding output port based on the arbitration result. Finally, the packet leaves the router.

III. LITERATURE REVIEW

Yuan, R.; Ruan, S.; Gotze, J. [1] Investigated on Network-on-Chip (NoC) be a new System on chip paradigm for the next generation for supporting a large number of processing cores. For achieving high computational throughput by a practical method without complex virtual channel or pipeline technology to provide high throughput (DES) Data Encryption Standard computation on FPGA. Results shows mesh-based NoC with packet and (PE) Processing Element design according to DES can achieve large performance than previous works.

Yoon Seok Yang, Jun Ho Bahn and Seung Eun Lee [2] presented the computational performance of NoC and multi-

processor system-on-chip for implementation of cryptographic block ciphers could be improved by parallel & pipeline execution work. This research work, a parallel and pipeline processing technique for block cipher algorithms: (DES) data encryption standard, (TDEA) triple-DES Algorithm, and (AES) advanced encryption standard based on pure software implementation on NoC.

Mahdoum, A., [3] worked on a new design methodology of a customized and distributed network on chip (NoC) that efficiently deals with either real-time or high throughput systems. The functional decomposition was achieved. A customized NoC is designed for each subsystem so that to avoid the hop count problem as the contention one while routing the packets from the source to the sink nodes.

Mahdoum, A., [4] estimated that the network on chip in order to meet the specific requirements of the involved application in terms of surface, the consumption and bandwidth. The numerous methodologies have been defined and are mainly based on mesh networks, fat trees and their variants. Author presented their synthesis method of the network architecture whose components (floor planning of the IPs, number and size of the interconnections) they are previously generated during design space exploration.
Mahdoum, A. [5] proposed an FPGA-like come up to on-chip communication where switches are avoided and two any IPs are connected if and only if when they are communicating. It avoids the difficulty of expensive intermediate hop counts of on-chip networks NOCs any two source-destination pairs. The temporal aspect of communication and then it is possible that some communication phases don't overlap; therefore a designer wants not provision resources for such cases.

Ruaro, M., Carara E.A. and Moraes, F.G. [6] Investigated the significant increase in the number of processing elements in NoC-Based MPSoCs, communication become, increasingly, a serious resource for performance gain and QoS guarantee the runtime adaptation of the NoC resources, consistent with the QoS necessities of every application running in the MPSoC. Authors performed the Monitoring and QoS adaptation implemented in software. Results with real applications reduced in average 60 percent the number of latency violations.

IV. PROBLEM IDETIFICATION

There are different kinds of problems arise during the routing process. Especially in oblivious routing this type of problem arises that result in blockage of traffic. The routing devices have to wait for the reduction of traffic and then try sending repeatedly. Deadlock, live lock and starvation are potential problems on both oblivious and adaptive routing.

Deadlock
The data packets are moving around the network, they reserve some resource in between the path. As all the packets are waiting for each other to release the resources in a cyclic way after that this kind of condition is called as deadlock. As a result the all packets will be blocked inside the deadlock condition and they may not be routed to their destination and that is a huge loss in the on chip networks.

Live lock

This difficulty happens while the packets are moving around a destination without reaching at destination. As a result data can’t be routed to the destination. This problem may happen in non-minimal routing algorithm where the routing algorithm choose the longest path whether the shortest path exist or not by observing the network congestion. For throughput improvement this problem shall be avoided.

Performance necessities that each NoC must satisfy

- Small latency
- Guaranteed throughput
- Path diversity
- Sufficient transfer capacity
- Low power consumption
- Fault and distraction tolerance
- Architectural requirements of scalability and programmability

V. CONCLUSIONS

In this review paper we have analyzed about many researches on Network on Chip (Noc). The necessities on communication in a system on chip follow the growing supplies on processing power closely. The communication systems cannot longer be taken for granted as the systems become more complex. From an analysis of the infrastructural context of modern chip designs, a network for on-chip use has been developed. This network can be designed with simplicity, giving small, area efficient and fast implementations of the network components. A speed-optimized implementation may be designed.

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