To Reduce The Power Dissipation of CMOS Logic Circuit Through Lactor Technique

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Abstract - Whenever we want to develop a digital integrated circuits, then we are facing a challenge by higher power consumption. The combination of greater functional integration, higher clock speeds and smaller process geometries have contributed to significant growth in power density. With the help of scaling we improves functionality on a chip, and transistor density. Scaling can also helps to increase speed and frequency of operation and hence higher performance. There are several techniques that can be use to reduce leakage power in efficient way but the main disadvantage of each technology that limits the application of each technique. In our base paper Dynamic CMOS circuits are significantly used in high-performance very large-scale integrated (VLSI) systems. And hear we are calculating static noise margin as well as noise analysis of this method However, they suffer from limitations such as noise tolerance, charge leakage, and power consumption. But in that paper they can ignored static power dissipation. Static power has become a great challenge for current and future technologies. There are many reasons for which power losses occur in CMOS circuit. 1) Sub-threshold leakage (weak inversion current) 2.) Gate oxide leakage (Tunnelling current 3.) Channel punch through 4.) Drain induced barrier lowering. Now, we can introduced a approach that can reduce the static power dissipation and leakage power dissipation of the circuit. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Now a day leakage power has become an increasingly very important issue. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are so many process technology and circuit-level solutions that can be used to reduced leakage. Now, we proposed a method that can used to reduced both leakage and dynamic power with minimum required area and delay.

Keyword- Micro-wind 3.0.

I. INTRODUCTION

In history of CMOS design, behind the speed and area of any chip, power dissipation or power consumption was secondary consideration. But however we are increasing the total number of transistors and clock frequency in a single chip, then power consumption comes in very serious issue. Instantaneous power drawn by any chip from the power supply is directly proportional to the multiplication of supply voltage v(t) and supply current $i_{dd}(t)$.

$$\mathbf{P(t) = i_{dd}(t)*v(t)}$$

Now, total energy consumed over some time interval T is,

$$\mathbf{E} = \int_0^T \boldsymbol{p(t).dt}$$

$$\mathbf{E} = \int_0^T \boldsymbol{idd(t).v(t)dt}$$

Now average power over this interval is,

$$\mathbf{P_{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T \boldsymbol{idd(t).v(t)dt}$$

There are mainly two components that establish the amount of power dissipation in a CMOS circuit, such as –

1) Static power dissipation

- Due to sub-threshold conduction,
- Tunnelling current through gate oxide,
- Leakage through reverse biased diodes,

2) Dynamic power dissipation

- Due to charging and Discharging of load capacitances,
- "Short circuit" current while both PMOS and NMOS networks are partially "ON"

Static power dissipation :

For static power dissipation we are considering the Static CMOS inverter which are shown in figure, If the input=0, the associated NMOS transistor is OFF and the PMOS transistor is ON. The output voltage is V_{dd} or logic 1. When the input =1 the associated NMOS transistor is ON and the PMOS transistor is OFF. The output voltage is 0 volt. Note that one transistor is always OFF when the gate is in either of these logic states. Ideally, no current flows through the

Off transistor so the power dissipation is zero when the circuit is quiescent. Zero quiescent power dissipation is a principal advantage of CMOS over competing transistor technologies. However, secondry effects including sub-threshold conduction, tunnelling and leakage lead to small amount of static current flowing through the "OFF" transistor. Assuming the leakage current is constant so instantaneous and average power are the same, the static power dissipation is the product of total leakage current and the supply voltage.

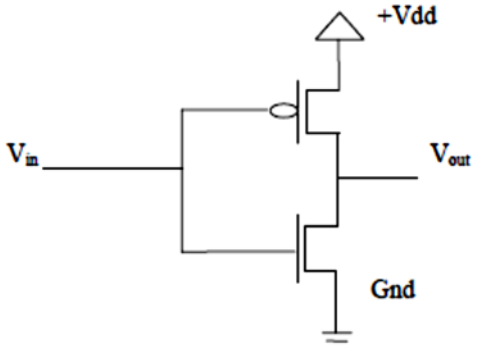


Fig 1.1 CMOS inverter circuit

$$P_{static} = I_{static} * V_{dd}$$

There is some small static dissipation due to reverse bias leakage between diffusion region and the substrate . in addition sub-threshold conduction can contribute to the static dissipation. Now we are introduced a model where we shows that the parasitic diode is shown between n-well and substrate. Since parasitic diodes are reverse-biased then only leakage current contributes to static power dissipation. The leakage current is described by the diode equation

$$I_o = i_s \left(e^{\frac{qv}{kt}} - 1\right)$$

Where i_s = reverse saturation current
V = diode voltage
Q= charge of electron ($1.602*10^{-19}$c)
K= Boltzmann's constant ($1038*10^{-23}$)
T = temperature

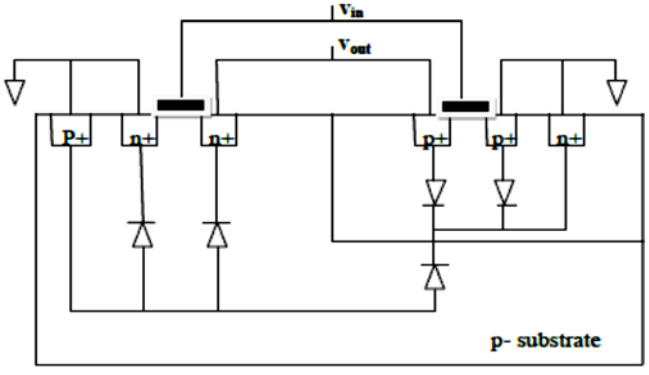


figure 1.2 Parasitic diode present in a CMOS inverter

The static power dissipation is the product of the devise leakage current and the power supply voltage.

$$P_{static} = \sum_{n=1}^{N} leakage\ current * \text{supply voltage}$$

Where n = number of devices.

II. PROBLEM STATEMENT

This research work is titled for to develop the area efficient VLSI design by reducing the static power through LACTOR technique. While designing a VLSI system power dissipation is one of the most important issue. Now, Up to a certain time dynamic power was the single largest concern but however the technology feature size shrinks static power has become an important issue as dynamic power. A well-known previous technique called the sleep transistor technique cuts off Vdd and/or GND connections of transistors to save leakage power consumption. However, when transistors are allowed to float, a system may have to wait a long time to reliably restore lost state and thus may experience seriously degraded performance. Therefore, retaining state is crucial for a system that requires fast response even while in an inactive state. The two common approaches are sleepy stack and sleepy keeper. Both methods are excellent in this regard. The static and dynamic power of sleepy stack is considerably low. But it has a delay penalty and its area requirement is maximum compared with other processes. Again the sleepy keeper process possesses excellent speed criteria but it requires more static and dynamic power than sleepy stack. Our goal is to trade off between these limitations and thus propose new methods which reduce both leakage and dynamic power with minimum possible area and delay trade off.

III. MOTIVATION

CMOS Technology was one of the main streams of VLSI Design. In 0.18u and above technology Dynamic power is one of the main factors of total power consumption. But when technology feature size shrinks to .13u and below technology static (Leakage) power dominates the dynamic power. So however, the designers proposed several methods to reduce the leakage.

In Base Technique there is a no method for power reduction but it saves the state as well as minimum area and delay. Sleep Transistor Technique is most common method for achieving ultra-low leakage but it destroy the state and as well as increasing delay and area. Forced stack technique is another method and it can save the state. But in this technique Dynamic Power consumption is increases and it cannot use high Vth without increasing the Delay. By combing these two

techniques Sleepy Stack approaches is proposed. It reduces the leakage similarly like sleep transistor technique but the main advantage over sleep transistor technique is save the logic state. Moreover, Sleepy Stack approach comes with area and delay overhead and slower method than other technique. However, Sleepy Keeper approaches are really appreciable for propagation delay and static power performances. Although, Sleepy Keeper approaches incurs area and dynamic power dissipation. But still now this two common technique is used. Hence we sought a new method which can have excellent trade off between power, area, and delay.

DESIGN CRITERIA

In present time we are mostly using CMOS Technology because of it's consuming less power. But time by time when technology feature size shrink sub-threshold leakage current is increases as the decrease of threshold voltage. In this design criterion we focused on sub threshold leakage power consumption and also focused on body biasing effect. Finally we explain the switching power and delay trade-off of generic CMOS circuit.

LEAKAGE

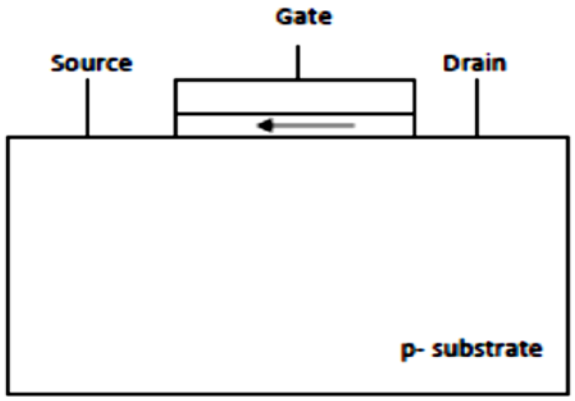


Figure 3.1 Sub-threshold Leakage of an NMOS

Whenever we are using 0.18u and above technology then dynamic power is the dominant factor but whenever we are using 0.13u and below technology then another dominant factor will be occurred that is called static power for power consumption. One of the main contributors for the static power consumption is sub-threshold leakage current which is shown in the Figure 3.1(a) i.e., the drain to source current when the gate voltage is small as compare to threshold voltage. When the size of the devices are decrease then sub-threshold leakage current is increases exponentially as the decrease of threshold voltage.

Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power. For turned off the single transistor in Figure 1.4 leakage current Isub0 can be expressed as follows:

$$I_{sub0} = A\, e^{1/nV\theta(Vgso - Vtho - \gamma Vsbo + \eta Vdso)}(1 - e^{-Vdso/V\theta}) \quad (1)$$

$$= Ae^{1/nV\theta(-Vtho + \eta Vdd)} \quad (2)$$

Where,

$$A = \mu_o C_{ox} (W/L_{eff}) V_o^2 e^{1.8}$$

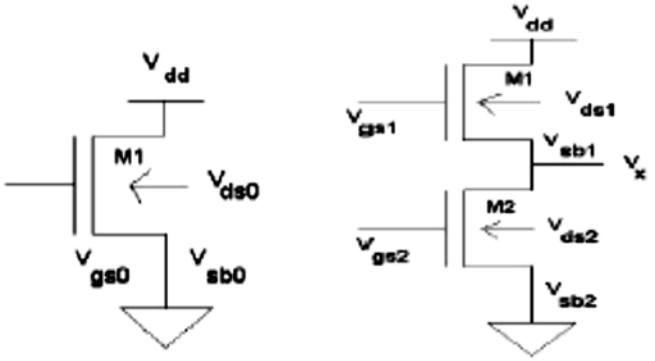


Figure 1.4 (i) Single Transistor (ii) Stacked transistor (iii) Stacked transistor

n=sub-threshold coefficient V_θ= thermal voltage V_{gs0}, V_{th0}, V_{bs0} and V_{ds0} are the gate-to-source voltage, the zero-bias threshold voltage, the base -to-source voltage and the drain-to-source voltage respectively. is the body-bias effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient. μ is zero-bias mobility, C_{OX} is the gate-oxide capacitance, W is the width of the transistor, and Leff is the effective channel length. (Note that throughout this project we assume μn = 2μp,i.e., NMOS carrier mobility is twice PMOS carrier mobility). Also note that we use a W/L ratio based on a actual transistor size, in which way a W/L ratio properly characterizes circuit models used in this case. In Figure two transistor are turned off together (M1=M2).So

$$I_{sub1} = A\, e^{1/nV\theta(Vgs1 - Vth0 - \gamma Vsb1 + \eta Vds1)}(1 - e^{-Vds1/V\theta}) \quad (3)$$

$$= Ae^{1/nV\theta(-Vx - Vtho - \gamma Vx + \eta(Vdd - Vx)} \quad (4)$$

$$I_{sub2} = A\, e^{1/nV\theta(Vgs2 - Vtho - \gamma Vsb2 + \eta Vds2)}(1 - e^{-Vds2/V\theta}) \quad (5)$$

$$= A e^{1/nV\theta(-Vtho+\gamma Vx)} (1-e^{-Vx/V\theta}) \quad (6)$$

Where Vx is the voltage at the node between M1 and M2, and we assume

$$1 >> e^{Vds1/V}$$

Now consider X is the factor of I_{sub0} and I_{sub1} (==I_{sub2})

$$X = \frac{Isubo}{Isub1} = \frac{e^{1/nV\theta(-Vtho+\eta Vdd)}}{e^{1/nV\theta(-Vx-Vtho-\gamma Vx+\eta(Vdd-Vx)}} = e^{Vx/nV\theta(1+\gamma+\eta)} \quad (7)$$

If I_{sub1}=I_{sub2} then equation (7) can written ,

$$1 = e^{1/nV\theta(nVdd-Vx(1+2\eta+\gamma))} + e^{-Vx/V\theta}$$

n coefficient will be increase as the technology feature size shrinks. Threshold voltage can be controlled by body bias effect.

$$V_{th} = V_{to} + \gamma(\sqrt{Vsb})$$

Changing the substrate voltage causes the threshold voltage to change. So the different kind of effect is arises for changing the substrate voltage like Zero-Body Bias, Reverse-Body Bias and Forward-Body Bias. This Phenomenon is frequently used for controlling the threshold voltage. constant dependent on the transistor parameter and the technology feature size. By controlling body biasing effect with changing the constant term we can easily control the leakage power.

IV. PROPOSED MATHEDOLOGY

The rapid progresses in semiconductor technology have leaded the feature sizes to be shrunk through the use of deep-submicron processes; thereby the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone.

To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device. The power dissipation has not diminished even with the scaling down of the supply voltage.

The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area has kept growing. For the rapid increase in power consumption of present day chips, the innovative cooling and packaging strategies are of little help. Also, the cost associated with the packaging and the cooling of such devices is becoming prohibitive. In addition to cost, the issue of reliability is a major concern. Component failure rate roughly doubles for every 10oC increase in operating temperature. With the on-chip devices doubling every two years, minimizing the power consumption has became currently an extremely challenging area of research.

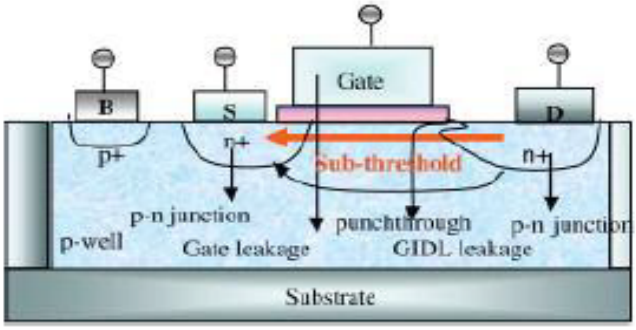


Figure 1.5 Static CMOS leakage sources

Leakage power of a CMOS transistor depends on gate length and oxide thickness. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure1.5.

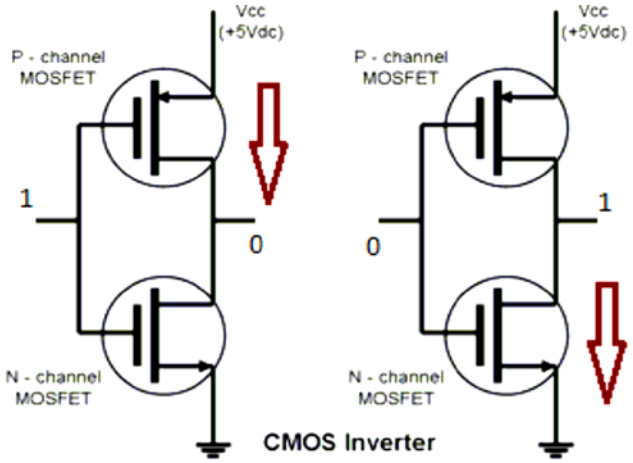


Figure 1.6 Reverse current in CMOS inverter

Sub-threshold leakage current; which is the reverse current flowing through the OFF transistor, indicated with arrows in Figure1.6. As the technology scales down which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated.

V. LECTOR TECHNIQUE

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from that "a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path". The number of OFF transistors is related to leakage power as shown in Figure1.7

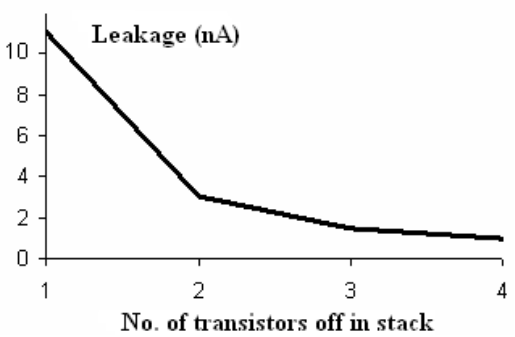


Figure 1.7 Transistor-stacking Vs Leakage Power.

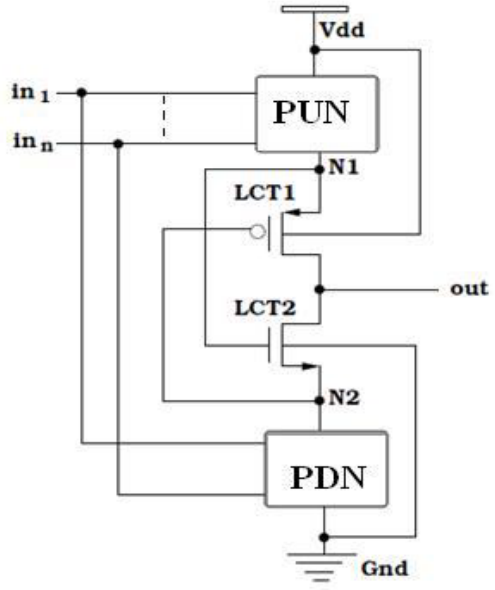


Figure 1.8 LECTOR CMOS Gate

In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cut-off region.

The topology of a LECTOR CMOS gate is shown in Figure 1.9. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

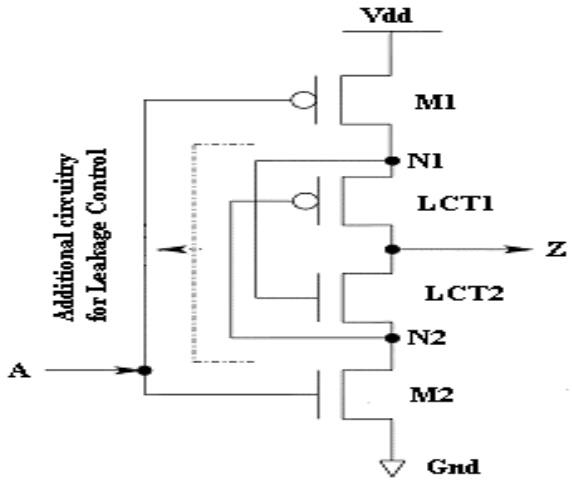


Figure 1.9 LECTOR based CMOS Inverter

Leakage Control Transistor (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Figure 1.9. A PMOS is introduced as LCT1 and a NMOS as LCT2 between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cut-off region for any input.

When Vdd = 1V, input A = 0, the voltage at the node N2 is 800 mV. LCT1 cannot be completely turned OFF as the voltage is not sufficient. Hence, the LCT1 resistance will be near to but slightly lesser than it's OFF resistance, allowing conduction. The resistance provided by LCT1, even though not equal to the OFF resistance, increases the resistance in the path of supply voltage to ground, thereby reducing the sub-threshold leakage current, attaining reduction in leakage

power. Similarly, when input A = 1, the voltage at the node N1 is 200 mV; hence LCT2 will be operated in near cut-off state. The states of all the transistors in the LECTOR inverter for all possible inputs are tabulated in Table I.

Along with the resistance in the path, the propagation delay of the gate also gets increased. The transistors of LCT inverter are sized such that the propagation delay is reduced or equal to its base case. In the sleep related technique, the sleep transistors have to be able to isolate the power supply and/or ground from the rest of the transistors of the gate. Hence, they need to be made bulkier dissipating more dynamic power. This offsets the savings yielded when the circuit is idle. Sleep transistor technique depends on input vector and it needs additional circuitry to monitor and control the switching of sleep transistors, consuming power in both active and idle states. In comparison, LECTOR generates the required control signals within the gate and is also vector independent. Two transistors are added in LECTOR technique in every path from V_{dd} to GND irrespective of number of transistors in pull-up and pull-down network.

TABLE I. STATE MATRIX OF LCT INVERTER

Transistor Reference	Input vactor (A)	
	0	1
M1	ON State	Off State
M2	Off State	ON State
LCT1	Near Cut- off State	ON State
LCT2	ON State	Near Cut- off State

Whereas, forced stacks have 100% area overhead. The loading requirement with LCTs is a constant which is much lower. Whereas, the loading requirements with forced stacks depend on number of transistors added and are huge. Hence, the performance degradation is insignificant in the case of LECTOR, and we overcome the drawback faced by forced stack technique.

APPLYING LECTOR TO CMOS CIRCUITS

Various circuit applications of the LECTOR technique are explored in this section. The LECTOR technique is applied to the following CMOS circuits and also their respective base case are implemented to calculate the amount of leakage power reduced in LECTOR technique.

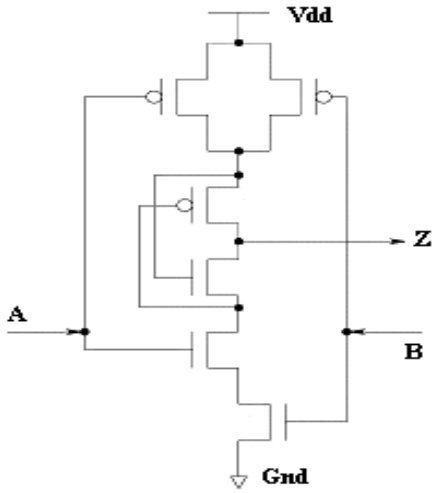


Figure 1.10 input LCT NAND

LECTOR based NAND gate

The 2-input CMOS NAND gate is shown in Figure 1.10 with the two LCTs added to pull-up and pull-down network between the V_{dd} and GND path. The simulation waveforms of LECTOR NAND from Figure 1.11 show that the basic characteristics of NAND are retained by LECTOR NAND.

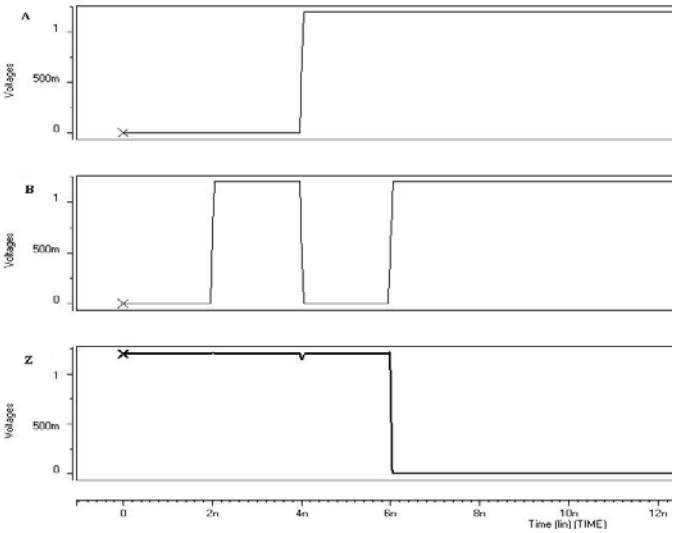


Figure 1.11 Simulation waveforms of LECTOR NAND

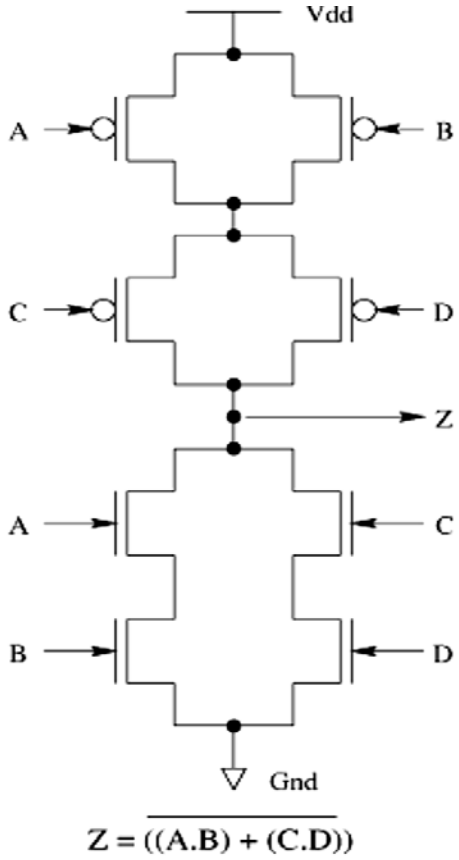


Figure 1.12 Four input AOI

4-input AND-OR-Invert

The SCCG (static CMOS complex gate) implementation of a 4-input AOI is shown in Figure 1.12 through which the area overhead can be reduced. The LECTOR implementation here needs only two additional transistors to be placed between the pull-up and pull-down network at the node from which the output is taken.

Figure 1.13 Simulation waveforms for LECTOR AOI

Through the simulation waveforms shown in Figure 1.13 the characteristics of LECTOR AOI resemble the base case.

4:1 Multiplexer

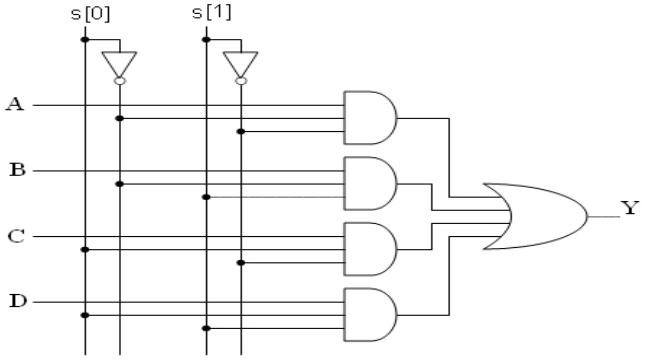


Figure 1.14 4:1 Multiplexer

The gate level schematic of 4:1 multiplexer is shown in Figure 1.14. The LECTOR implementation involves the addition of two LCTs in each gate between the supply and ground path.

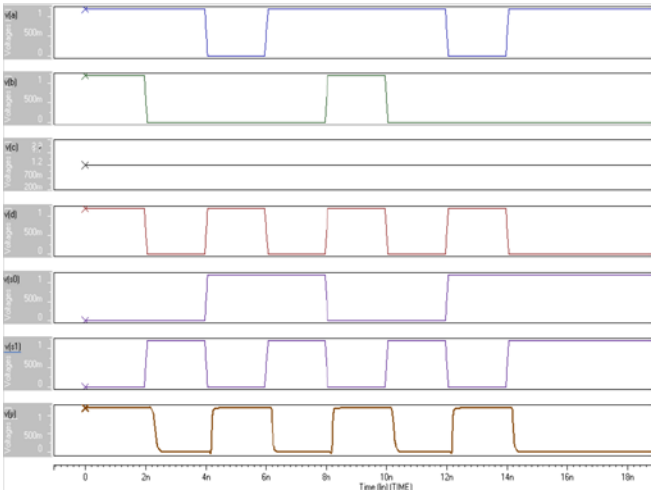
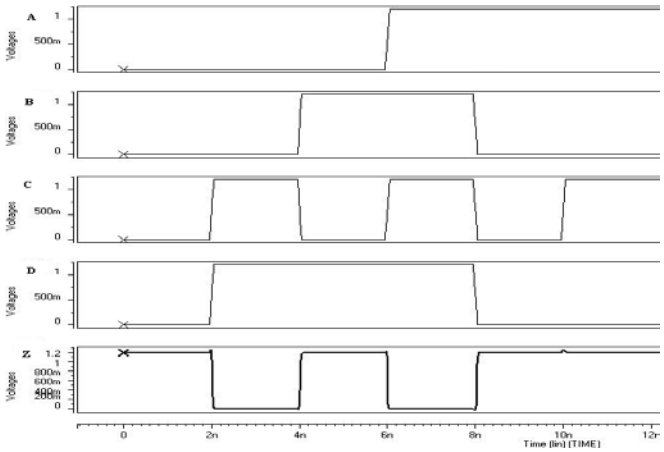


Fig. 1.15 Simulation waveforms for LECTOR MUX



The simulation waveform shown in Figure 1.15 represents the LECTOR Multiplexer through which it can be observed that its characteristics resemble that of the conventional case.

Full Adder

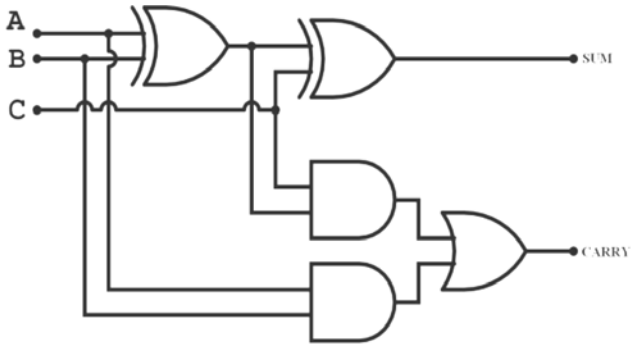


Figure 1.16 A Full Adder

The Gate level schematic of Full Adder is shown in Figure 1.16. The LECTOR implementation involves the addition of two LCTs for each gate. The transistor level schematic for ex-or gates is similar to that of And-Or-Invert.

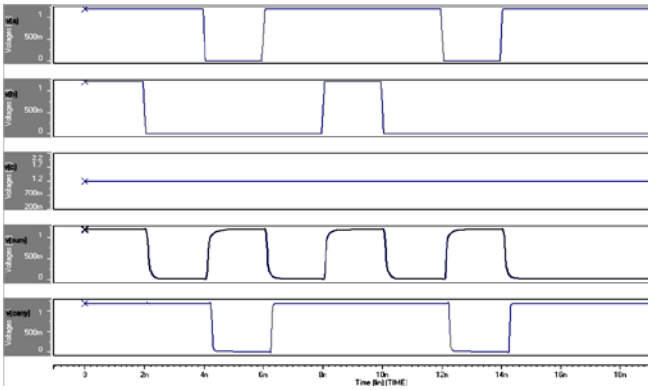


Figure 1.17 Simulation waveforms for LECTOR Full Adder

The simulation waveforms for full adder as shown in Figure 1.17, resembles the characteristics of conventional full adder.

VI. EXPERIMENTAL RESULTS

The leakage power is measured using the HSPICE simulator. The results obtained through the technique for 2-input NAND gate is shown in Table III. Simulation for the 2-input NAND is performed by taking four different process parameters Viz. 180nm, 90nm, 65nm and 45nm.

TABLE II. SUPPLY VOLTAGES AND THRESHOLD VOLTAGE VALUES

Tecnology	180nm	90nm	65nm	45nm
Supply voltage	1.8V	1.2	1.1	1
NMOS V (Volt)	0.3999	0.2607	0.22	0.1777
PMOS V (Volt)	-0.42	-0.303	-0.22	0/1156

The supply voltages to be considered for the four process parameters (technologies) along with the threshold voltages for NMOS and PMOS in the respective technologies are as shown in Table II.

Table III gives the results for 4-input AOI for 90nm and 45nm technologies. Table IV gives the results for 4:1 Multiplexer and Full Adder under 90nm process parameters.

TABLE III RESULT FOR 4-INPUT AOI

Data Sheet		4-input AOI	
		90nm	45nm
leakage Power (W)	CONVENTIONAL	3.76E-09	2.13E-06
	LECTOR	2.45E-09	1.65E-06
Percentage decrease in Power Dissipation		34.914	22.223

TABLE IV RESULT FOR 4:1 MULTIPLEXER AND FULL ADDER

Data Sheet		4:1 MUX	Full Adder
		90nm	45nm
leakage Power (W)	CONVENTIONAL	3.76E-09	2.13E-06
	LECTOR	2.45E-09	1.65E-06
Percentage decrease in Power Dissipation		34.914	22.223

Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. There are 4 possible combinations for 2-input NAND, hence the average of the four power dissipations gives the leakage power. In the case of 4-input AOI, power dissipations corresponding to all the 16 combinations are averaged. For Multiplexer, the average of 64 power dissipations is considered and for full adder, the average of 8 power dissipations is considered to be as the static power dissipated. In each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with same set of input vectors.

VII. REMARK

The increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nano-meter technologies and thus it becomes a great challenge to tackle the problem of leakage power. LECTOR uses two LCTs which are self-controlled transistors. LECTOR achieves the reduction in leakage power like other leakage reduction techniques, such as sleepy stack, sleepy

keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LECTOR technique when applied to generic logic circuits achieves up to 40-45% leakage reduction over the respective conventional circuits without affecting the dynamic power. A trade off between Propagation delay and area overhead exists here as the delay reduction by sizing the transistors will increase the area overhead.

VIII. CONCLUSIONS

The increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nano meter technologies and thus it becomes a great challenge to tackle the problem of leakage power. LCPMOS uses one LCT which is controlled by the output of circuit itself. LCPMOS achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LCPMOS technique when applied to generic logic circuits achieves up to 80-92% leakage reduction over the respective conventional circuits without affecting the dynamic power. A trade off between Propagation delay and area overhead exists here.

CMOS technology in nano-meter scale faces great challenge due to sub-threshold leakage power consumption. The earlier approaches and our proposed approaches can be effective in some ways, but no one exactly knows the real solution for the reduction of power consumption. So, based on different technology and design parameters the techniques are chosen by the designers. The earlier approaches are discussed in brief in this paper and two novel approaches are proposed for generic logic and memory circuit. The methods can be applied to single and multi-threshold voltages. The proposed methods are unique in area saving and faster than any other approaches. Trade-off between power and delay is occurred in excellent way in our methods. So, these stacked sleep, variable body biasing and forced sleep techniques represent a new way in the VLSI designer's working area.

IX. SUGGESTIONS FOR FUTURE WORK

When we are analysing static power dynamic power and propagation delay then we are using MICROWIND. Again for area calculation we used MICROWIND. Static power, dynamic power and propagation delay are dependent on threshold voltage (V_{th}) and temperature variation can be also estimated in these all methods.

In future, we are proposed a new methods that can be implemented for 1-bit adder, low power pipelined cache etc. In future we are also calculating static noise margin as well as noise analysis of this method.

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