An Analysis on Reversible Logic Gates for Efficient VLSI Design

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Abstract- In this review paper we reviewed that the Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Many researchers provide advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs a 2*2 Swap gate which is a reduced implementation in terms of quantum cost and delay to the previous Swap gate is presented. Next, a novel 3*3 programmable UPG gate capable of calculating the fundamental logic calculations is presented and established, and its advantages over the Toffoli and Peres gates are discuss. The UPG is then implemented in a reduced design for calculating n-bit AND, n-bit OR and n-bit ZERO calculations. The UPG and RC are implemented in the design of novel sequential and tree-based comparators. Then, two novel 4*4 reversible logic gates (MRG and PAOG) with minimal delay, and may be configured to create a variety of logical calculations on fixed output lines based on programmable select inputs lines. Then, reversible implementations of each research paper are analyzed and compared.

Keywords: Index Terms Arithmetic Logic Unit (ALU); Reversible Logic; Quantum Computing.

I. INTRODUCTION

Reversible logic is a promising computing design paradigm which presents methods for constructing computers that produce no heat dissipation. Reversible computing emerges as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Particularly, the fundamentals of reversible computing are based on the relationship. The possibility of a quantum particle occupying a particular state at any specified time, and the quantum electrodynamics between electrons when they are in close proximity.

The fundamental principle of reversible computing is that a objective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every probable state, resulting in no heat dissipation.

II. ARITHMETIC LOGIC UNIT

An ALU is a critical component of a microprocessor [1] and is the core component of central processing unit. In addition, it is the heart of the instruction execution portion of every computer. An ALU is a multi-functional circuit that conditionally performs one of several possible functions on two operands *A* and *B* depending on a selection input. A one bit conventional ALU that performs four operations viz., one arithmetic (addition) and three logical (AND, OR and XOR) operations is shown in Fig. 1 in which a 4 to 1 multiplexer is used to select one of the specified four operations by means of two selection inputs S_0 and S_1, and its functional table is given in table 1. In a classical design of ALU (Fig. 1), arithmetic and logical operations are first performed in parallel and then the desired result is selected by a multiplexer. All other results are lost. This destructive approach is suitable for conventional Boolean circuits because it uses large number of gates with more garbage outputs. In the following sub sections, we focus on the design of a reversible ALU that can be part of a programmable reversible computer.

A. Multiplexer based reversible ALU

Similar to conventional ALU, a reversible ALU can be realized using a multiplexer to select one of the ALU operations. In this work, two different ways, type I and type II realization of an ALU using reversible gates are proposed, in either of which a 4 to 1 multiplexer is used to select one of the operations.

This ALU is simple to design and verify because it consists of several independent sub circuits. As it is parallel, it is expected to be fast, but this comes at the cost of a large logic width and more number of constant inputs.

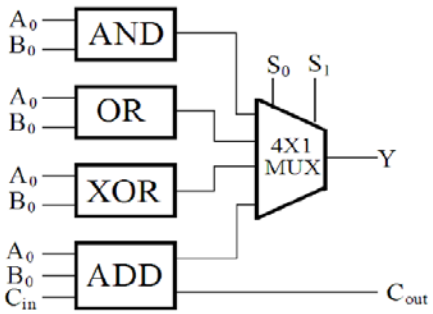


Fig. 1. One bit conventional ALU

B. Control Structure Based Reversible ALU

The control structure based reversible ALU can be expected to be slower because of a larger logic depth and is more complex to design than a parallel ALU because of more involved control, but has a smaller logic width. The reduced number of constant inputs is also consistent with our goal of having a minimal design. An ALU design for more difficult arithmetic instructions may benefit from a combination of the parallel and sequential designs (possibly using constant inputs). The addition of control to a reversible circuit is an essential and necessary transition to form the next, advanced level of control in a reversible computing system that integrates many elementary controlled gates (e.g. Fredkin, Toffoli and Feynman gates) into a more complex controlled system. This could be compared to the addition of control to an elementary logical operation on a lower system level, such as $\oplus$, to obtain an elementary controlled logic gate, say a Feynman gate, apart from the design of the functionality and control of an entire unit is more complex. In this work, to perform ALU operations five control signals are used.

TABLE II. COMPARISON OF TYPE I AND TYPE II ALUS

Parameter	Type I	Type II
Gate count	9	7
Garbage outputs	6	5
Quantum cost	34	30
Quantum depth	34	26
Constant inputs	5	4
Logical calculation	16α+19β+8γ	16α+16β+6γ

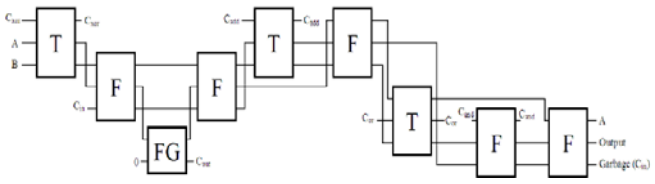


Fig. 2. Control structure based reversible one bit ALU

To make the circuit to be reversible all the control signals are made to appear at the output. Depending on the control signal, the output is produced and is available on the B input line as shown in Fig. 2. Another input A is also produced at the output.

Fig. 2 shows reversible ALU that is based on control inputs and its quantum representation is shown in Fig. 2. From these figures it is clear that the circuit has one constant input, five control inputs and one garbage output.

III. REVERSIBLE LOGIC GATES

There are three basic 2x2 reversible logic gates. The Controlled-Not gate [2] commonly called the Feynman gate - is designed to produce the following output states: $P = A$ and $Q = A \oplus B$. Since fanout is expressively forbidden in reversible logic, since a fanout has one input and two outputs, the Feynman gate can be used to duplicate a signal when B is equal to 0.

Fig. 3: Quantum Representation of Feynman Gate

A Reversible Arithmetic Logic Units

A reversible arithmetic logic unit was designed by Thomsen, Glück, and Axelsen [3] that was based on the V-shaped design of the Van Rentergem adder [4]. The ALU had five fixed select lines, and formed the following logical outputs: ADD, SUB, NSUB, XOR and NOP. The least significant bit comprised of two Feynman gates and two Toffoli gates. Each extra bit also had two Fredkin gates.

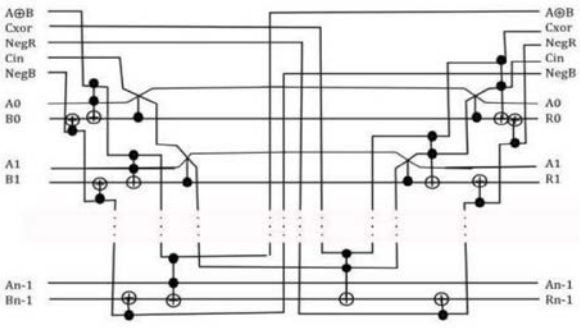


Fig. 4: Reversible ALU Presented by Thomsen

B Reversible ALU Design with MRG and PAOG

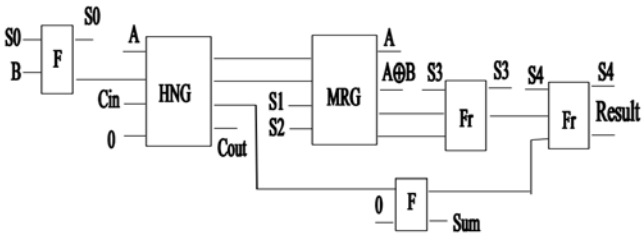
Two 1-bit ALUs are presented in this section. The first utilizes the MRG gate and HNG gate to produce six logical calculations: ADD, SUB, XOR, XNOR, OR and NOR. The ALU has 8 inputs and 8 outputs. The inputs consist of three data inputs (A, B and Cin) and five fixed input select lines. The eight outputs are: A, S0, S3 and S4 propagated to the output, A ⊕ B, SUM, Cout, Overflow and Result. The cost of this 1-bit ALU is 24, and the worst-case delay is 16. For n-bit ALU devices, an addition cost of 2 is incurred per bit in order to propagate S1 and S2 to other bits. Therefore, the total cost for an n-bit ALU is 26 n-2. The proposed ALU is shown in Fig. 15, and the logical results based on the input opcodes are presented in Table 2.

Table 2 ALU Op codes and Logical Result for Fig.5

S4	S3	S2	S1	S0	Result
0	0	0	0	0	XOR
0	0	0	1	0	=
0	1	0	0	0	OR
0	1	1	0	0	NOR
1	0	0	0	0	ADD
1	0	0	0	1	SUB

Figure.5: Reversible ALU with MRG and HNG Gates

The second ALU utilizes the PAOG gate and HNG gate to produce six logical calculations: ADD, SUB, AND, NAND, OR and NOR.



The cost and delay calculations are identical to the ALU in Fig. 3. The proposed ALU is shown in Fig. 6, and the logical results based on the input op codes are presented in Table 3.

S4	S3	S2	S1	S0	Result
0	0	0	0	0	AND
0	0	0	1	0	NAND
0	1	0	0	0	OR
0	1	1	0	0	NOR
1	0	0	0	0	ADD
1	0	0	0	1	SUB

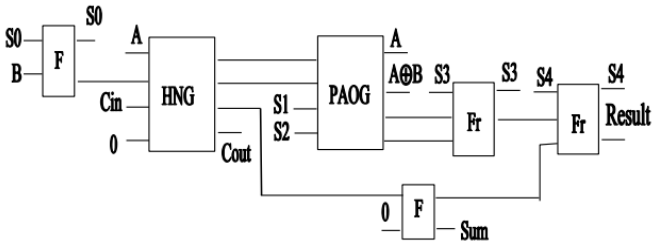


Fig.6: Reversible ALU with MRG and HNG Gates

IV. Relevant Works And Literature Review

In the previous work the ALU had five fixed select lines, and produced the following logical outputs: ADD, SUB, NSUB, XOR and NOP with the delay of 470ns. The fundamental physical concepts behind reversible logic. Four specific aspects of reversible logic design. First, the fundamental reversible logic gates. Next will be discuss reversible arithmetic, specifically adders and comparators. Next, the previously proposed ALU in the literature. Finally, the two previously presented reversible comparators.

Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan *"Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder"*[7]
In this work we present the all optical implementation of an n bit reversible ripple carry adder for the first time in literature. The all the optical reversible adder design is based on two new optical reversible gates referred as optical reversible gate I (ORG-I) and optical reversible gate II (ORG-II) and the existing all optical Feynman gate. The proposed all optical reversible ripple carry adder will be a key component of an all optical reversible ALU that can be applied in a wide variety of optical signal processing applications.

Matthew Morrison, Matthew Lewandowski, and Richard Meana, *"Design of a Novel Reversible ALU using an Enhanced Carry Look-Ahead Adder"*[10]
In this research work reversible logic gate is presented and confirmed, and its implementation in the design of a reversible Arithmetic Logic Unit is showed. Then, reversible

implementations of ripple-carry, carry-select and Koggestone carry look-ahead adders are analyzed and compared. Further, implementations of the Kogge-Stone adder with sparsity-4, 8 and 16 are designed, verified and compared. The enhanced sparsity-4 Kogge-Stoneadder with ripple-carry adders was selected as the top design, and its implemented in the design of a 32-bit arithmetic logic unit is demonstrated

Y. Syamala and A. V. N. Tilak, *"Reversible Arithmetic Logic Unit*" [9]
The control unit based ALU is developed with 9*n* elementary reversible gates for four basic arithmetic logical operations on two *n*-bit operands. The sequences of operations are performed on the same line depending on control signals, in the place of selecting the desired result by a multiplexer. The presently design is found to be advantageous over the former in terms of number of garbage outputs and constant inputs produced.

Anindita Banerjee, *"Reversible cryptographic hardware with optimized quantum cost and delay*"[11]
We have proposed novel designs for reversible ALU of a cryptoprocessor which have been implemented in standard gate library and the quantum cost reported here are better than the lower bounds reported in literature. Additionally we have calculated delay of the proposed designs. We have verified that designs are minimal with respect to gate count which is circuit cost by simulating it in Rev Kit. This is for the first time that the optimization algorithms to optimize quantum cost and delay have been applied to improvise on the cost metric in reversible ALU design.

Bibhash Sen, Manojit Dutta, Debajyoty Banik and Dipak K Singh "Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA"[8]
This work targets design of reversible ALU (arithmetic logic unit) in QCA (Quantum-dot Cellular Automata). The design is based on the reversible QCA structure (RQCA) introduced in this research paper. A fault tolerant architecture of reversible ALU is also synthesized. The designs are verified and evaluated over the existing ALU designs and found to be more efficient in terms of design complexity and quantum cost.

V. CONCLUSION

Here it can be concluded that the fundamentals of reversible computing are based on the relationship entropy, heat transfer between molecules in a system, the prospect of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity.. In future we can have some other combination of reversible logic gates that is MRG and HNG gates that provides more arithmetic and logical operations and hence delay can be reduced to some more extent. Apart from that if the delay reduces power also is reduced. The concept of a programmable reversible logic structure and theorems were proposed that introduce new metrics for reversible logic design. Next, a 3x3 reversible UPG gate was presented and verified which is was a functional improvement on the Peres Gate, and gave an improved quantum cost and delay over the Toffoli gate, and is able to produce all the desired logical outputs – AND, NAND, OR, NOR, without any additional logical structures.

REFERENCES

[1] Y. Syamala and A. V. N. Tilak "Reversible Arithmetic Logic Unit",2011 IEEE

[2] R. Feynman, "Quantum Mechanical Computers," Foundations of Physics, vol. 16,iss. 6, 1986.

[3] M. Morrison, M. Lewandowski, R. Meana and N. Ranganathan, "Design of Static and Dynamic RAM Arrays Using a Novel Reversible Logic Gate and Decoder," To Appear in the IEEE 11th International Conference on Nanotechnology, 2011.

[4] M. Morrison and N. Ranganathan, "Design of a Moore Finite State Machine using a Novel Reversible Logic Gate, Decoder and Synchronous Up-Counter," To Appear in the IEEE 11th International Conference on Nanotechnology, 2011.

[5]. R. Feynman, "Simulating Physics with Computers," *International Journal of Theoretical Physics*, 1982.

[6]. J. Smolin and D. Divincenzo, "Five Two-bit Quantum sGates Are Sufficient to Implement the Quantum Fredkin Gate," *Physical Review A*, vol. 53, 1996, pp 2855-6

[7] Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan, "Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder" 2012 IEEE.

[8] Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh, Biplab K Sikdar, "Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA" 2012 International Symposium on Electronic System Design.

[9] Y. Syamala, A. V. N. Tilak, "Reversible Arithmetic Logic Unit", 2011 IEEE.

[10] Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan, "Design of a Novel Reversible ALU using an Enhanced Carry Look- Ahead Adder" , 2011

11th IEEE International Conference on Nanotechnology Portland Marriott August 15-18, 2011, Portland, Oregon, USA

[11] Anindita Banerjee , “Reversible cryptographic hardware with optimized quantum cost and delay” 2010 Annual IEEE India Conference (INDICON).

[12]. H. Thapliyal and M. Srinivas, "Novel Reversible 'TSG' Gate and Its Application for Designing Components of Primitive Reversible/Quantum ALU," *Tenth Asia-Pacific Computer Systems Architecture Conference*, 2005.

[13]. M. Shams, M. Haghparast and K. Navi, “Novel Reversible Multiplier Circuit in Nanotechnology”, *World Applied Sci. J.*, Vol. 3, pp. 806- 810, 2008.

[14]. M. Haghparast, S. J. Jassbi, K. Navi and O. Hashemipour, “Design of a Novel Reversible Multiplier Circuit using HNG Gate in Nanotechnology ”, *World Applied Sci. J.*, Vol. 3, pp. 974-978, 2008.

[15]. S. Islam, M. Rahman, Z. Begum, and M. Hafiz, "Realization of Novel Fault Tolerant Reversible Full Adder Circuit in Nanotechnology," *The International Arab Journal of Information Technology*, vol. 7, iss. 3, 2010, pp 317-333.