A Novel Reduction Technique For Wallace Multiplier Reduction

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Abstract - Power dissipation of integrated circuits is a major concern for VLSI circuit designers. A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses carry save addition algorithm to reduce the latency. This paper proposes new reduction method that is the use of half adders is greatly reduced and the full adders is increased, than the standard Wallace multipliers. As half adders does not reduce the partial product bits the delay in both modified and the conventional Wallace is kept the same. As a result the circuit complexity is reduced by 20% and Power Consumption is reduced by 10%.

Keywords - Multiplier, Wallace, Power Consumption, VLSI Circuits.

1. INTRODUCTION

A multitude of various multiplier architectures have been published in the literature, during the past few decades. The multiplier is one of the key hardware blocks in most of the digital and high performance systems such as digital signal processors and microprocessors. With the recent advances in technology, many researchers have worked on the design of increasingly more efficient multipliers. They aim at offering higher speed and lower power consumption even while occupying reduced silicon area. This makes them compatible for various complex and portable VLSI circuit implementations. However, the fact remains that the area and speed are two conflicting performance constraints. Hence, innovating increased speed always results in larger area[2]. The conventional and modified Wallace reduction multipliers have three stages in their reduction process. First stage, the product matrix of N x N is formed when two N bit numbers are multiplied. The second stage, N x N product matrix is reduced to a product of two terms. In the third stage, the two terms are added with a carry propagating adder to generate the final product. This paper is concerned with the second phase where the N rows of partial product bits are reduced to two rows. In this stage, the Wallace approach uses several stages of full and half adders to maximize the reduction at each stage. Full adders take in three bits and output is of two bits for a net reduction of one bit per full adder. Half adders take in two bits and output two bits. They simply shift the position of one of the bits.

2. PREVIOUS WORK

For the conventional Wallace reduction method, once the partial product array (of N2 bits) is formed, adjacent rows are collected into non overlapping groups of three. Each group of three rows is reduced by 1) applying a full adder to each column that contains three bits, 2) applying a half adder to each column that contains two bits, and (3) passing any single bit columns to the next stage without processing. This reduction method is applied to each successive stage until only two rows remain.

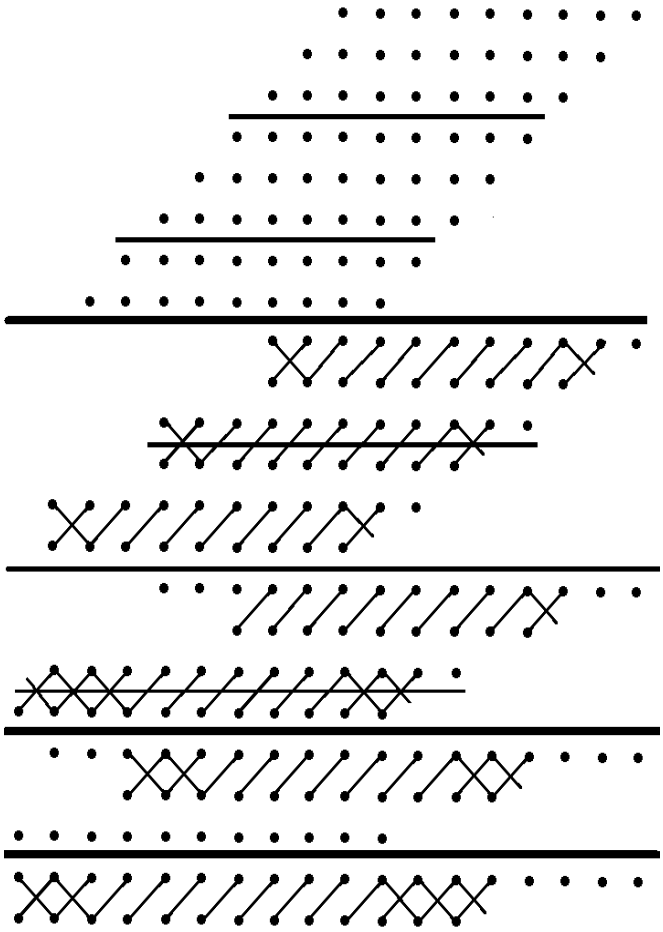

Fig.1.Conventional Wallace 9-bit by 9-bit reduction.

The final two rows are summed with a carry propagating adder. This process is illustrated by the conventional 9-bit by 9-bit Wallace multiplier shown in Fig. 1. Light lines show the three row groupings. The reduction is performed in four stages (each with the delay of one full adder) with a total of 50 full adders and 21 half adders. The third phase will require a 13-bit wide adder.[1]

3. MODIFIED WALLACE

This section presents the modified Wallace method for reducing the partial product array (the second phase). As shown in Fig. 2, the initial partial product array of the first phase is changed by shifting bits in the left half of the array upward to form an inverted pyramid array (the partial product generation method is the same, no data are changed; only their vertical position is shifted). In the second phase, the modified Wallace approach is similar to the conventional Wallace approach in that it uses as many full adders as possible, but different in that it only uses half adders when necessary to ensure that the number of reduction stages is the same for the conventional Wallace multiplier[3]. The modified Wallace reduction method divides the matrix into three row groups and uses full adders for each group of three bits in a column like the conventional Wallace reduction. A group of two bits in a column is not processed, that is, it is passed on to the next stage (in contrast to the conventional Wallace reduction). Single bits are passed on to the next stage as in the conventional Wallace reduction. The only time half adders are used is to ensure that the number of stages of the modified Wallace multiplier does not exceed that of a conventional Wallace multiplier[4]. For some cases, half adders are only used in the final stage of reduction. In the 9-bit by 9-bit example, a half adder is used in the first and the second stages to handle partial product terms that, if not addressed, would increase the number of reduction stages and increase the multiplier delay. Also two half adders are used in the final stage. The reduction is performed in four stages (the same as the Wallace reduction) with a total of 52 full adders and four half adders. The third phase will require a 16-bit wide adder. The modified Wallace reduction uses two more full adders and 17 fewer half adders than the conventional Wallace reduction.

4. CONFIGURATION DETAILS

For an N-bit multiplier, the number of rows in the initial bit product array, r_0, is N. The number of rows in subsequent stages of a conventional Wallace multiplier is

$$r_{i+1} = 2[r_i/3] + r_i \bmod 3 \quad \text{---------- (1)}$$

$$\text{If } r_i \bmod 3 = 0, \text{ then } r_{i+1} = 2[r_i/3] \text{---------- (2)}$$

where, y mod z denotes the smallest nonnegative remainder of y/z. For a 9-bit by 9-bit multiplier, the stage heights given by (1) are: $r_0 = N = 9$, $r_1 = 6$, $r_2 = 4$, $r_3 = 3$, and $r_4 = 2$.

Therefore, four stages are required for the reduction. As seen in the reduction of the 9-bit by 9-bit modified Wallace multiplier shown in Fig. 2, without the half adder in the first stage, the second matrix would have seven rows instead of the six that are required for the conventional Wallace reduction.

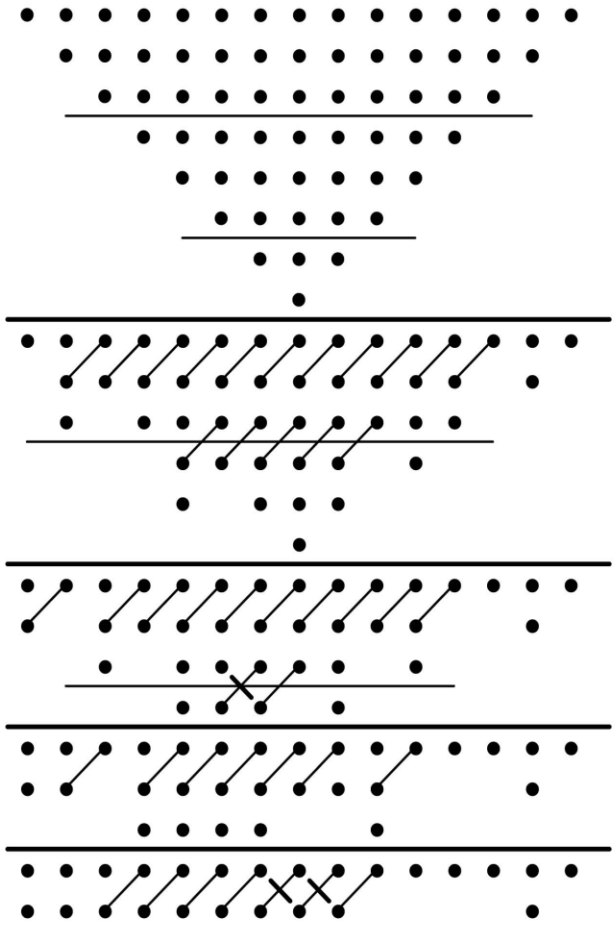

Fig.2.Modified Wallace 9 bit by 9 bit reduction.

5. EXPERIMENTAL RESULTS

Conventional 9x9 wallace multipliers

The total number of half adder used in the second stage is 21.

The total number of full adders used in the second stage is 43.

Modified 9x9 wallace multipliers

The total number of half adders used in the second stage is 3.

The total number of full adders used in the second stage is 37.

6. CONCLUSION

The Wallace approach uses several stages of full and half adders to maximize the reduction at each stage. Full adders take in three bits and output is of two bits for a net reduction of one bit per full adder. Half adders take in two bits and output two bits. By using this method the no of half adders is reduced by 20% which leads to reduced circuit complexity and power consumption is reduced by 10%.

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