Design for Testability for Mixed Launch and Capture Power Reduction Based on Scan Chain Reordering

Neethy V[1], Raghu M.C[2]
[1]PG Scholar, [2]Assistant Professor

Abstract

Testing of digital VLSI circuits has many challenges as a consequence of rapid growth of semiconductor manufacturing technology. These challenges include keeping the test power and the delay produced within acceptable limits. Here proposed design for testability (DfT) support along with scan chain reordering for enabling the use of a set of patterns optimized for cost and quality as is, yet in a low power manner. Mixed testing of Launch off shift and Launch off capture operation can be performed to get higher fault coverage. Reordering of these scan chains significantly reduces the test power and delay while testing.

Keywords

Design for testability, scan chain reordering, mixed testing, Low power

1. Introduction

Testing of sequential circuits has been one of the most challenging areas in digital circuits. Automatic test generation for large sequential circuits without Design for Testability logic has met with marginal success. Power consumption during testing is much higher than during normal circuit operation. It is important and essential to target low power dissipation during testing, since excessive heat can damage the circuit under test.

Generally a circuit may consume more power in the test mode than normal mode. The main reasons behind these are following: First, DfT circuitry can be embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in the test mode. Second, the test efficiency has a high correlation with the toggle rate; hence, the switching activity of all nodes is often several times higher than the activity during normal operation. Third, in SoC, parallel testing is reduce test time, which result in excessive energy and power dissipation. The test power may be responsible for several kinds of problems like instant circuit damage, decreased system reliability, performance degradation and decrease of overall yield.

A technique can be used to reduce the test power is the scan chain reordering. In scan chain reordering algorithm, some cells of the ordered scan chain will be reordered again in order to reduce the test power. The reordered cells in the scan chain minimize the hamming distance between the test vector and the captured response in the test cycle, hence reducing the capture power. A test power reduction frame work for LOS based and LOC based at speed testing and scan chain reordering can be proposed to reduce the test power.

2. System Model

The system model consists of LFSR, Test and benchmark circuit with LOS/LOC circuit. It is used to support the test methodology. So, the power can be reduced. Another power reduction method can applied in the circuit using scan chain reordering. The transaction count is less then speed can be improved. Test power and speed performance can be improved by using mixed testing circuit. Further the system model can be improved by scan chain reordering.

3. Previous Work

LOS and LOC testing could unambiguously find faults during reciprocally exclusive manner. A mixed test with LOS and LOC patterns can yield higher fault coverage level compared to either testing scheme applied alone. [1]

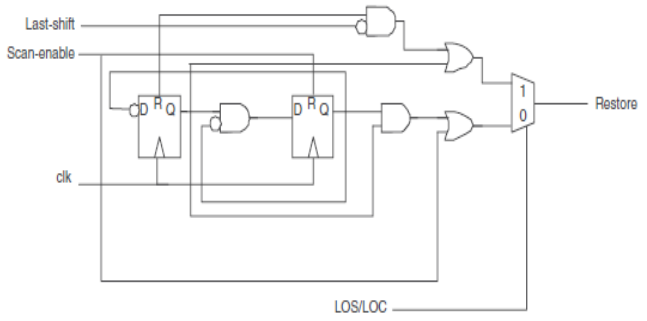

Fig.1: Restore generation circuit

LOS/LOC signal that denotes the type of test for the pattern applied instantly and can be controlled by programmable register bit (No need for additional pin), can make the correct selection of signal.

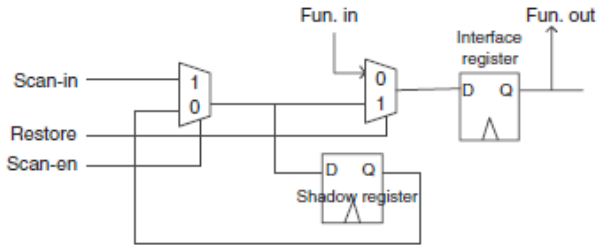

Fig.2: Mixed test circuit

To support each low power LOS/LOC testing Figure 1 can be utilized. According to the selection signal of the LOS/LOC the restore signal can be get at the output section in Figure 1. Restore signal selects the output of the mixed test circuit. The combinational circuit output is given to the mux through the Fun. in input [2].[3]. The registers are used to store the value for detecting the fault.

4. Proposed Methodology

Test methodology consists of LFSR, Test module with scan chain reordering circuit and benchmark circuit with LOS/LOC circuit.

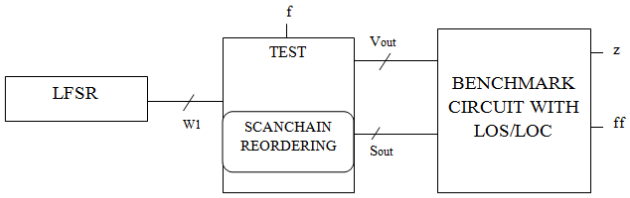

Fig.3: Block diagram of Test methodology

Linear feedback shift register (LFSR) is used to generate the test patterns to the circuit under test. The output W1 is given to the test module. The test module is used to divide the output data in benchmark circuit and scan chain and also used for scan chain reordering. Vout is the input to the benchmark circuit and Sout is the input to the scan chain. By using mixed testing circuitry, the benchmark circuit can be tested. The output of benchmark circuit is given as z. The ff output is the functional output of the LOS/LOC testing circuit and also the vector of scan chain. f is the response vector of test module and used for scan chain reordering.

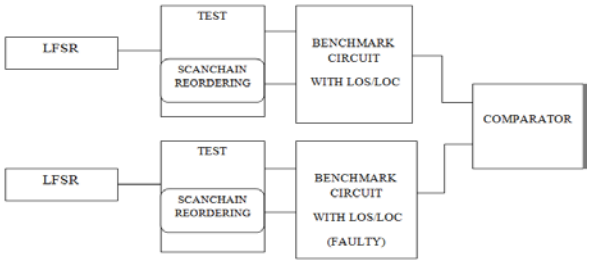

Fig. 4: Test circuit

Fig.4 shows the test circuit of this technique. It consists of LFSR, Test with scan chain reordering and benchmark circuit with LOS/LOC technique. One circuit is faulty and another one is a good circuit. Both outputs are given to the comparator and outputs are verified. The faults can be identified using the output of comparator.

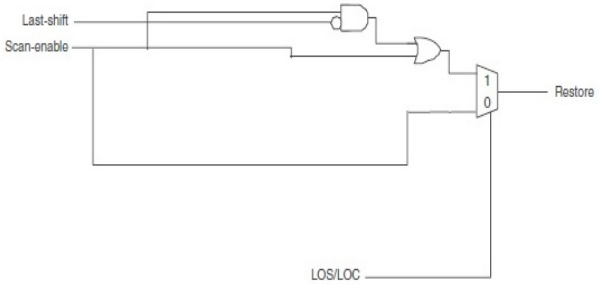

Fig. 5: New Restore generation circuit

Figure 5 shows the new Restore generation circuit. It reduces the area of the circuit. It uses last-shift, scan- enable and LOS/LOC signals.

5. Simulation/Experimental Results

The test methodology architecture is synthesized in Spartan 2E starter board as the evaluation development board. The family is Spartan 2E, the device used is XC2S600E, the

package is FG676 and the speed is -6. The top level source type is HDL, the synthesis tool is XST (VHDL/Verilog), and the simulator is ISE Simulator (VHDL/Verilog). Simulation can be done by using Model sim software. Power analysis can be done by X Power analysis in Xilinx ISE 8.1i. The power analysis of LOS/LOC and the scan chain reorder as follows;

Table-1: Actual parameter values of s208 circuit

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.8		
Dynamic		92.94	167.30
Quiescent		15.00	27.00
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Power			200.90
Startup Current		500. 00	

The s208circuit values are given above. The startup current is 500 mA and the Vccint is 1.8V.The total power is 200.90mW.The total delay of s208 circuit is given as 7.655ns

.Table-2: HTML Power Report of s208 circuit

Power summary	I (mA)	P (mW)
Total estimated power consumption		201
Vccint 1.80V:	108	194
Vcco33 3.30V:	2	7
Clocks:	85	152
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	4	7
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

The HTML Power Report of s208 is shown in Table 2. The maximum frequency used in s208 circuit is given as 130.634MHz.Minimum input arrival time before clock is 7.655ns.Maximum output required time after clock is 13.496ns.

Table-3: Actual parameter values of s208 LOS/LOC

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.8		
Dynamic		71.01	127.81
Quiescent		15.00	27.00
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Power			161.41
Startup Current		500. 00	

The actual parameter values of s208 LOS/LOC circuit are given below. The voltage is shown in V, the current in mA and the power in mW. The startup current is 500 mA and the Vccint is 1.8V.The total power is 161.41mW. The delay performance is given in ns. The total delay of s208 LOS/LOC circuit is given as 6.490ns.

Table-4: HTML Power Report of s208 LOS/LOC

Power summary	I (mA)	P (mW)
Total estimated power consumption		161
Vccint 1.80V:	86	155
Vcco33 3.30V:	2	7
Clocks:	63	113
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Table-5: Actual parameter values of scan chain reordering s208 circuit

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.8		
Dynamic		64.37	115.87
Quiescent		15.00	27.00
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Power			149.47
Startup Current		500. 00	

The HTML Power Report of s208 LOS/LOC circuit is shown in Table 4. The current is given in mA and the power in mW. The Vccint is 1.8V and the total estimated power consumption is 161 mW. The maximum frequency used in s208 LOS/LOC circuit is given as 154.083MHz.Minimum input arrival time before clock is 5.1222ns.Maximum output required time after clock is 12.996ns.

The actual parameter values of scan chain reordering of s208 circuit are given below. The voltage is shown in V, the current in mA and the power in mW. The startup current is 500 mA and the Vccint is 1.8V.The total power is 149.47mW. The delay

performance is given in ns. The total delay of scan chain reordering of s208 circuit is given as 6.290ns.

Table-6: HTML Power Report of scan chain reordering s208 circuit

Power summary	I (mA)	P (mW)
Total estimated power consumption		149
Vccint 1.80V:	79	143
Vcco33 3.30V:	2	7
Clocks:	56	101
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Table-7: Comparison of Benchmark circuits

Circuit		P(mW)	Delay(ns)	Area
s27	Normal	132	4.902	244
	LOS/LOC Method	113	3.704	70
	Scan chain reordering	108	3.504	38
s208	Normal	201	7.655	1034
	LOS/LOC Method	161	6.490	574
	Scan chain reordering	137	5.852	340
s298	Normal	221	7.020	1132
	LOS/LOC Method	162	6.744	773
	Scan chain reordering	129	4.624	190

The HTML Power Report of scan chain reordering of s208 circuit is shown in Table 6. The current is given in mA and the power in mW. The Vccint is 1.8V and the total estimated power consumption is 149 mW. The maximum frequency used in scan chain reordering of s208 circuit is given as 158.983MHz.Minimum input arrival time before clock is 7.327ns.Maximum output required time after clock is 13.596ns.

The experimental result of various benchmark circuits as follows. It shows that scan chain reordering can reduce the area, delay and test power. Area can be in total equivalent gate counts for design.

6. Conclusion

The proposed DfT support for mixed testing based on scan chain reordering can reduce the launch and capture power in the design regions. Therefore a set of patterns optimized for cost and quality can be utilized also in low power manner. This technique offers the advantage of reduction in test power, significant improvement in speed and reduction in area. The design also offers the advantage of simplicity and required minimum design effort.

Scan chain reordering technique can be simulated using Model sim and power analysis and speed performance can be synthesized and analyzed by using Xilinx ISE software. From the power analysis it can be viewed that the power consumption of s208 is 201mW.The total power consumption of s208 LOS/LOC circuit is given as 161mW. After scan chain reordering it can be 149 mW. The delay performance of s208, s208 LOS/LOC circuit and s208 after scan chain reordering is given as 7.655ns, 6.490ns and 6.290ns respectively. Hence it is clear that total power consumption, delay and area can be reduced to a great extend using scan chain reordering.

7. Future Scopes

As future work, compression techniques are used. The main advantage of compression technique is reducing test data and test time. Use PODEM algorithm instead of Automatic test pattern generator (ATPG).

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Author's Profile

Neethy V has received her Bachelor of Technology degree in Electronics and Communication Engineering from Jawaharlal college of Engineering and Technology in the year 2013. At present she is pursuing M.Tech in VLSI Design at Nehru College of Engineering and Research Centre, Thrissur. Her areas of interest include Communication, Low power design and VLSI.

Raghu M C has completed ME in VLSI Design from KCG college of Technology, Chennai under ANNA University. At present he is working as an Assistant Professor at Nehru College of Research and Engineering, Pampady, Thrissur. His areas of interests are VLSI, Digital IC Design.