Parallel Counter Architecture of Transmission Gate Base Flip Flops Divided by N Pre Scalar Counter

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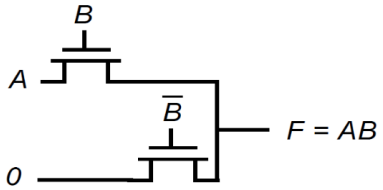
Abstract Instead of using conventional counter design technologies, a decision logic circuit is needed to generate predictable counting states. In order to attain high operating frequency a high-speed parallel counter is presented. In our work the counter operating frequency is varied by using a parallel counter architecture of transmission gate base flip flops. The operation speed is improved by reduction of the critical path delay and the low power consumption is due to a smaller number of interconnects. The counter can be used as a frequency divider circuits. Each flip flops divide the input clock frequency by two. For generation of different clock frequencies, different counter structures are designed. Reduction in number of transistors will reduce the number of inter connect. The use of transmission gate also reduces number of stray capacitances and interconnect length, which in turn reduces the interconnect delay and power dissipation. In this work the structure of counter composes of three simple CMOS logic modules. An initial module generates predictable counting states for higher significant bit modules through the state look- ahead path. In order to attain high operating frequency a high-speed parallel counter is presented.

I. INTRODUCTION

The microprocessor, microcontroller and digital signal processor base systems operates on different frequencies. The counter is use as frequency dividers. Counter generate



clocks of different frequencies. The n bit cascaded counter counts 2^n states and is called as divide by 2^n counter. These states are called as modulus of counter. The divide by N counter is the mostly usable module for frequency synthesizers. The circuit propose in this work consist of area and power optimize flip flops with an extra logic which determines the terminal counts and the step size of counting for generation of different frequencies. The circuitry is design is mainly focused on the reduction of complexity of design so that the different frequencies are possible to generate without any design complexity. The transmission gate base Delay flip flop design with 12 transistors as compare to conventional flip flops of 36 transistors. The circuit is design with multiplexer logic structure of transmission gate instead of cross connected NAND gate structure. A popular and widely used alternative to complementary CMOS is pass transistor logic. Pass transistor logic attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals.

Figure 1.1: Pass Transistor logic base AND Gate

1.2 Transmission Gate Base Counter Design:

Our design counter circuits can be built using T flip-flops because the toggle feature is naturally suited for the implementation of the counting operation. We can design this flip fop by connecting the ON output to the D input of Master slave D flip-flop shown in a figure 4.7. Figure shows four bits counter capable of counting from 0 to 15. The clock inputs of the four flip-flops are connected in cascade. The input of each flip-flop will be toggled at each negative edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary in

II. LITERATURE REVIEW

In a low voltage and low power divide by N/N+1 counter is design using pass transistor logic technique. A counting and mode selection logic is design with a single transistor in this work with reduced critical path between flip flops. The divider achieves high-speed operation using a novel parallel counter and a pipelined architecture. The parallel counter is based on a state look-ahead component in conjunction with an internal pipeline structure in order to simultaneously trigger all state value updates without a rippling effect. In a digital CMOS high-speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology is design using state look ahead path logic. It consists of three design modules.

Saleh Abdel-Hafeez, and Ann Gordon-Ross publish their work on title "A Digital CMOS Parallel Counter Architecture Based on State Look-Ahead Logic" in IEEE Transactions on Very Large-Scale Integration (VLSI)

Systems, Vol. 19, No. 6, June 2011 pp no 1023. In their work they present a high-speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology (a counting path and state look-ahead path), using only three simple repeated CMOS-logic module types: an initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path, simple D-type flip-flops, and 2-bit counters. Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance were enabled when all bits in all modules of lower significance (containing lower significant bits) saturate. Initializations and propagation delays such as register load time.

2.2 Problem Formulation

Frequency dividers are widely considered as a major limiting factor in frequency synthesizer systems, which require a very fast settling frequency feedback loop and a wide-range of frequency division ratios. Among the most important parameters of high-speed dividers are the operating frequency, operating range, and power consumption. Most modern frequency dividers are typically classified as cascaded asynchronous programmable presale counters, programmable swallow counters, or programmable divide-by-N counters. The counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using pass transistor circuit design techniques. In our work the counter operating frequency is varied by using a parallel counter architecture of pass transistor base flip flops.

III PROPOSED METHODOLOGY

3.1 Transmission Gate:

For this implementation we can use transmission gate logic. Transmission Gate has the capability of a high-quality switch with small resistance and capacitance. Transmission gate is the part of our design module. The delay of the transmission gate can be modelled by linearized RC network.

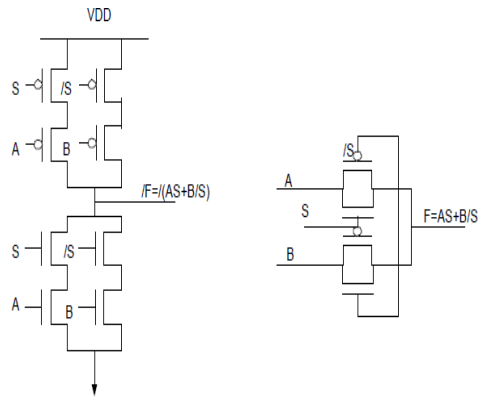


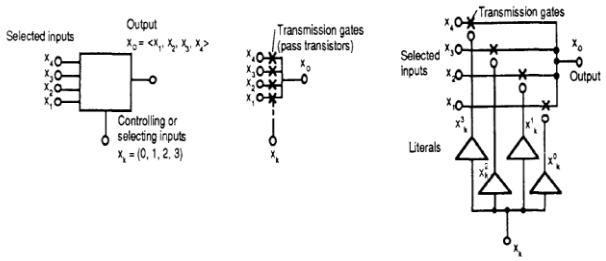
Figure 3.1: Transmission Gate base quadrature value logic.

The on-resistance and diffusion capacitance of transmission gate is represented by a resistor. Transmission Gate is generally used to implement of XORs and MUXs with the minimum number of transistors.

3.2 Architecture Design

The architecture designs of our adder logic consist of transmission gate (TG) base multiplexer logic. Here the full adder is design by using transmission gate base OR, AND, XOR logic gates. Figure 3.3 shows the transmission gate base OR gate. When input enable is equal to logic '0' then it will transmit input B towards V_{out} by upper TG otherwise it will transmit input logic '1' towards V_{out} by lower TG.

$$t_p = 0.69 \sum_{i=1}^{N} C_i \left(\sum_{j=1}^{i} R_j \right),$$



Schematic design for CMOS and TG base multiplexer logic

3.3 Propose Parallel Counter Architecture:

The Parallel counter is design with three basic modules consists of flip-flops and extra logic, which determines the next state of counter. The counter structure consists of these three design modules counts succeeding states through a fixed set of preassigned count states, of which each subsequently count state represents the successive counter value in a chain.

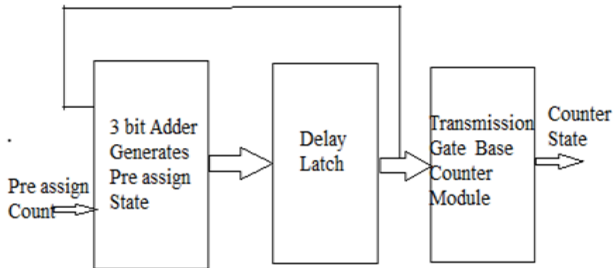


Figure 3.7: Block diagram of parallel counter

The transmission gate base counter design modules consist of three modules called as adder module, latch module, and counter module. This module determines the next state of counter depends on the present state i.e. design modules counts succeeding states through a fixed set of pre-assigned count states, of which each subsequently count state represents the successive counter value in a chain.

The input clock of multiplexer module is connected to the different counter circuits through transmission gate base de-multiplexer. This logic can be extended for more divide by N counter using higher size DE multiplexer logic. The 16 states counter module is design with a transmission gate base multiplexer logic circuit which work as a 16 states counter logic.

3.4 Power Reduction

The power dissipation in MOSFET is

$$P_{avg} = P_d + P_{sc} + P_{leak} + P_{static}$$

Where, P_d is the capacitive switching power dissipation, P_{sc} is the short-circuit power dissipation, P_{leak} is the power dissipation due to leakage currents and P_{static} is the static power dissipation due to non-leakage static currents. Capacitive switching power and short-circuit power are components of dynamic power dissipation. Leakage power is a major component of static power dissipation in CMOS circuits. dynamic power dissipation of a digital CMOS circuit depends on the supply voltage V_{dd}, the clock frequency f_{clk}, the node switching time, the node capacitances, the node short circuit current and the number of nodes. A reduction of each of these parameters results in a reduction of dissipated power. The dynamic power can be reduced by reducing capacitive load which is generated from gate, diffusion and interconnect wiring. This can be done by using pass transistor transmission gate logic which reduces number of transistors and interconnect nodes as possible.

3.5 Design Flow

Functional description is primarily studied and the structure of the digital IC circuit to be designed. Behavioral description is then formed to analyze the design in terms of functionality, performance, compliance to given principles, and other specifications.

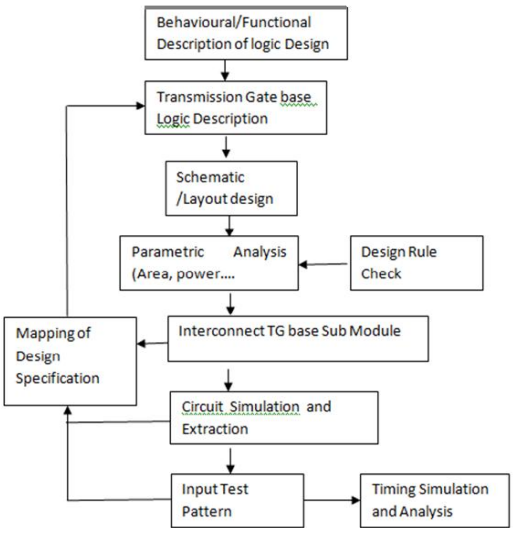


Figure 4.1: Implementation Logic Design Flow

RTL description is made by the use of Micro wind layout editor tool. This layout description is simulated to analysis functionality. From here forwards work needs the help of layout simulator tools.

3.6 Design Modules

The very large-scale integrated circuits (VLSI) operates on different number of clock frequencies. The N number of states in counter can be measured as MOD-N or divide by N counter. Each cycle of counter consists of N number of states. The circuit propose in this work consist of area and power optimize flip flops with an extra logic which determines the terminal counts and the step size of counting for generation of dissimilar frequencies.

IV SIMULATION RESULT & CONCLUSION

Simulation Result :- MICROWIND supports entire front-end to back-end design flow. For front-end designing, we have DSCH (digital schematic editor) which posse's in-built pattern-based simulator for digital circuits.

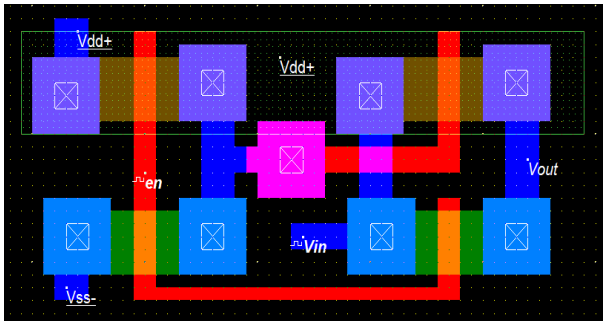
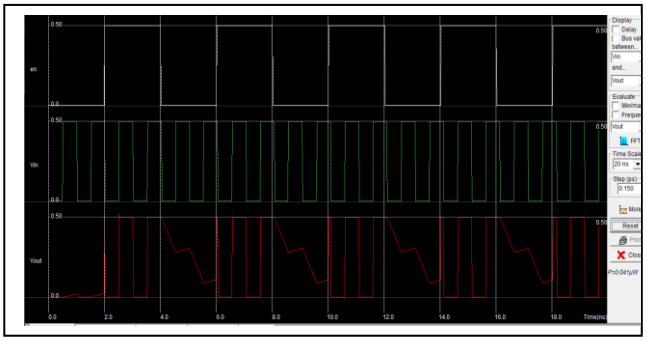


Figure 5.1: CMOS Layout Design For Transmission gate



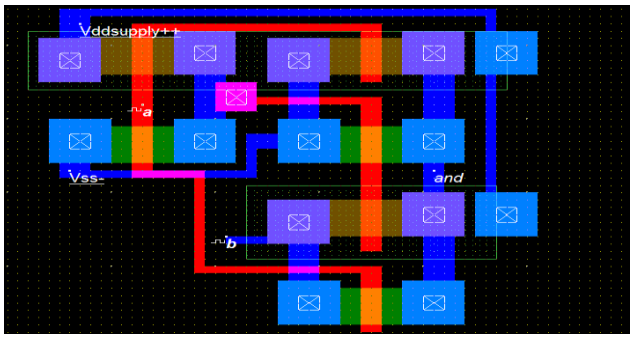


figure 5.2: Timing Simulation For Transmission gate

User can also build analog circuits and convert them into SPICE files and use 3rd party simulators like Win Spice or p--SPICE. DSCH can convert the digital circuits into Verilog file which can be further synthesized for FPGA/CPLD devices of any vendor. The same Verilog file can be compiled for layout conversion in MICROWIND.

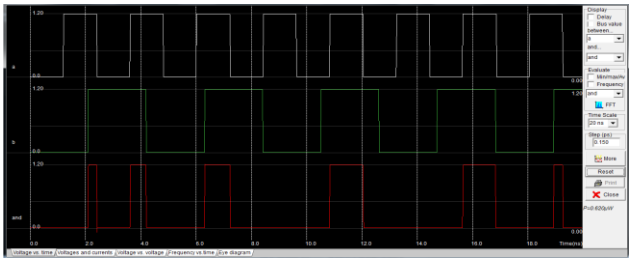


Figure 5.3: CMOS layout Design for Transmission gate base AND Logic Gate.

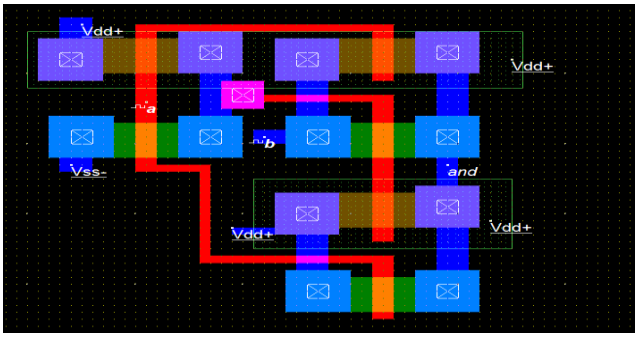


Figure 5.4: Timing Simulation of Transmission gate base AND Logic Gate

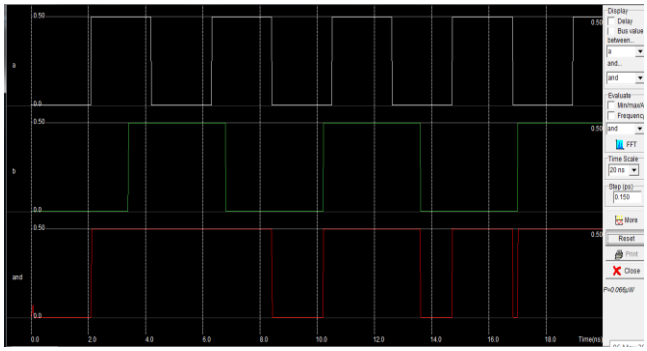


Figure 5.5: CMOS layout Design for Transmiision gate base OR Logic Gate.

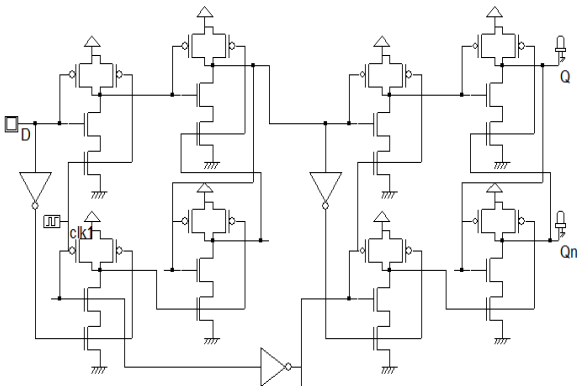


Figure 5.6: timing Simulation of Transmiision gate base OR Logic Gate

4.1 Comparative Analysis

S. No.	*Parameters*	*Conventional Results*	*Our Work*
1	Transistor Size (µm)	0.18um	0.05um
2	Number of transistors	13	45
3	Layout Area (µm)	71.98	14.35
4	Average Power (µW)	4.35/4.61	2.03
5	Switching Delay (µs)	1.88/1.9	0.03
6	PDP	8.19/8.78	0.05

V CONCLUSION

Frequency dividers are widely considered as a major limiting factor in frequency synthesizer systems, which require a very fast settling frequency feedback loop and a wide-range of frequency division ratios. Among the most important parameters of high-speed dividers are the operating frequency, operating range, and power consumption. Most modern frequency dividers are typically classified as cascaded asynchronous programmable pre scaler counters, programmable swallow counters, or programmable divide-by-N counters. The counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using pass transistor circuit design techniques. In our work the counter operating frequency is varied by using a parallel counter architecture of pass transistor base flipflops. The design is implemented on 50nm technology. The area of design is 15.375 um which is less as compare to previous work as the transistor size is shrink to 0.05um. The average power dissipation is 1.013uW.

VI FUTURE SCOPE

Frequency divider is one of the important blocks for a variety of circuit operations which is widely used in many applications such as radar, digital communication, and electronic imaging. A frequency divider is use to divides the frequency of the input signal by N to obtain the output frequency at 1/N times the input frequency. Counter is design for low-power and high-speed applications such as radar and digital communication.

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