Performance Analysis of Cascaded Multi-level Inverter Fed Induction Motor

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Abstract – Today's multilevel inverters have become very important topology for ac drives. Multi-level voltage source inverter technology has emerged as an important alternative in the control of high power medium voltage energy. The main purpose of this paper is to compare different cascaded multilevel inverter fed induction motor. This paper also describes the comparison between harmonics distortion values, a voltage and current waveforms of induction motor. More over it can also be used for charged balance controlled amongst the multiple input DC sources in a given topology multilevel voltage source inverters have various advantages: Reduction in electro-magnetic interference, reduction in the voltage rating of the power semiconductor switching devices, for better output voltage having reduced total harmonic distortion. Here we analysis the different firing scheme for cascade H-Bridge multilevel inverter.

Keywords – Cascade H-Bridge multilevel inverter, Total harmonic distortion (THD), CPWM, PD, POD, AOPD, Induction motor.

I. INTRODUCTION

In recent year many industrial drive use ac induction motor because induction motor is less expensive and reliable generally induction motor is used for constant speed but now a day's induction motor is also used for variable speed with the help of power electronics devices. These electronics devices not only improve the speed of motor but it can also improve the steady and dynamic characteristics of motor. There are various schemes such as PWM, SPWM, SVPWM, CPWM. etc. for controlling multilevel inverter like diode clamp inverter, capacitor clamp inverter, cascading H-bridge multilevel inverter for achieving dynamics performance of induction motor. In this paper we use cascade H-Bridge multilevel inverter for controlling induction motor.

1) It produce output voltage with low distortion and lower dv/dt .
2) They draw input current with very low distortion.
3) It generates smaller common mode voltage for reducing the stress of the motor load.
4) It can operate with a lower switching frequency.

In recent year industry require higher power which is reached in megawatt. For working with higher voltage we introduce multi-level inverter to control ac drives. Such as diode clamp inverter, capacitor clamp inverter and cascaded H-Bridge multilevel inverter. In this paper we briefly discuss about cascaded H-Bridge multi level inverter.[1],[6]

II. CASCADE H-BRIDGE MULTILEVEL INVERTER

Cascade H-Bridge multilevel is better than other multi-level inverter because its structure is simple. It requires less switching components. Cascade H-Bride multilevel inverter is the group of capacitor and switches.[15]

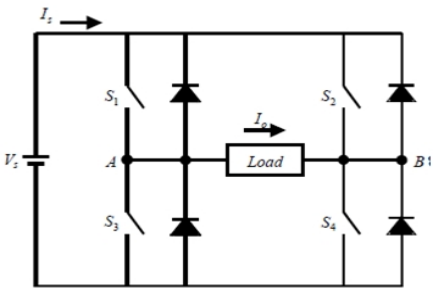

Fig. 1 Cascading H-Bridge MLI

In the above fig1. The circuit diagram of cascading H-Bridge multilevel inverter. Cascading H-Bridge multi level inverter is most important topology in the multilevel inverter. It gives a desire AC voltage from several DC input voltage it require less number of component as compare to diode clamp inverter and flying capacitor inverter each H-Bridge multilevel inverter produce three level of voltage Vdc, 0, -Vdc by different combination of four switches S1, S2, S3 and S4 .then the magnitude of ac output voltage will be.

$$V0 = V01+V02+V03+Von \text{ ---------- (1)}$$

Switching pattern of cascade H-Bridge multilevel inverters shown below.

Table no. 1 Switching table for cascade H-Bridge MLI

V0 = Van	S1	S2	S3	S4
Vdc	1	0	0	1
0	1	1	0	0
0	0	0	1	1
- Vdc	0	1	1	0

Cascaded N-level inverter:

A cascaded N-Level inverter consist of a number H-

Bridge inverter with separate dc source for each unit and connected in series as shown in fig.2. Each h-Bridge can be produce three level of voltage namely +Vdc, 0, and -Vdc.

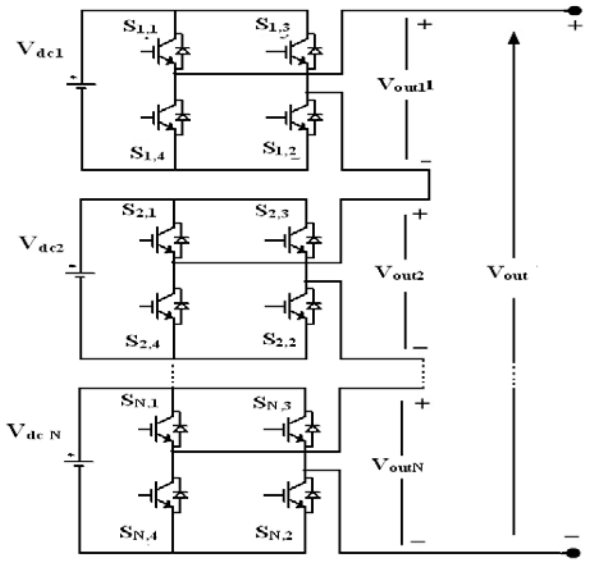

Fig2. Block diagram of cascaded N-Level inverter

For symmetric inverter all dc voltage sources equal to Vdc, the number of available voltage step level is:

$$N_{step} = 2n + 1 \text{---------- (2)}$$

Where n represented the number of full-bridges and maximum output voltage will be:

$$V_{omax} = n \times Vdc \text{---------- (3)}$$

There are following advantage of cascading H-Bridge multilevel inverter:

(1)It reduces total harmonic distortion.

(2)It requires less number of components for each level.

(3)It is more flexible than other multilevel inverter.

(4)Its circuit is simple and reliable.

Disadvantage:

The main disadvantage of cascading H-Bridge multi inverter is it requires separate DC voltage sources.

III. CONTROL SCHEME FOR MULTILEVEL INVERTER

There are following method for controlling the multi level inverter discussed below.

(a)Pulse width modulation technique (PWM).

(b)Sinusoidal Pulse width Modulation(SPWM).

(C)Third harmonics pulse width modulation (THI-PWM).

(d)Space vector pulse width modulation (SPPWM)

(e)Selective Harmonic Elimination Method (SHE-PWM).

Pulse width modulation control:-

This method is most popular method of controlling the output voltage, in this method a fixed dc input voltage is given is given to the inverter and controlled ac output voltage is obtained by adjusting the off periods of the inverter components. [17-19]

There are following advantage of pulse width modulation

(1) The output voltage control with this method can be obtained without any additional components.

(2) With this method lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized.

Space vector pulse width modulation:

In a conventional two level multilevel inverter the harmonics reduction in the output current of inverter is computed by increasing the switching frequency however in high power applications the switching frequency of the power device is restricted below 1kHz because of increasing switching losses and level of dc voltage. While the very high dv/dt which is generated with high DC link voltage is the cause for electromagnetic interference and motor winding stress. There for from the harmonic reduction and high DC – link voltage level point of view multilevel inverters are more suitable.

Much has been worked on the space vector modulation of multilevel inverter. In SVPWM method the output voltage is presented in three dimensional Euclidean space. The principle of this method is that increase in the number of level by one allows forms and additional hexagonal rings of equilateral triangles which surrounds the outermost hexagon. The hexagon which represent space vector diagram is flatten and reference voltage vector is normalize so that the computation of the algorithm is reduce.

A SVPWM has a predictive current control loop in this load the current is determined for all output voltage vectors of the inverters. The calculation of current error and selection of switching state is done when the value of error is less. A SVM causes reduction in the inverter output voltage distortion because of turn OFF , turn ON and dead times of power modules without increasing the harmonics content.[9-11],

The reference vector can be written as

$$V = (T_1 V_n + T_2 V_{n+1})/T_s \text{----------(4)}$$

Whereas T_1, T_2 are applied effective times corresponding to the active vectors $V_1 – V_6$.

The effective time can be calculated as follows

$T_1 = VT_S \sin(\pi/3-\alpha) / Vdc2/3 \sin(\pi/3)$ ------- (5)

$T_2 = VT_S \sin(\alpha) / V_{dc}2/3 \sin(\pi/3)$ ---------- (6)

$T_0 = T_s - T_1 - T_2$ ---------- (7)

Where T_0 is the time corresponding to null vector V_{dc} is the DC linkage voltage and T_s is the sampling time.

Multicarrier Sine–PWM :-

Multilevel carrier based PWM method have triangular waves or saw tooth waves multiple carrier signals show freedom in following characteristics – frequency, amplitude, face of each carrier and offset between the carriers. The reference wave can be either sinusoidal or trapezoidal. A reference wave two shows freedom in parameters like frequency, amplitude, phase angle, and injection of zero sequence signal to it. Hence many multilevel carrier based PWM methods, using these combinations may be obtained.[27], [33],

The carrier based Schemes can be classified as:

(a)Level shift PWM (LSPWM)

(b)Phase shifted PWM (PSPWM)

(C)Hybrid (H)

Level shift PWM

(1)Alternative phase opposition disposition (APOD) – In alternative phase opposition disposition the carrier signals are out of phase by 180°.

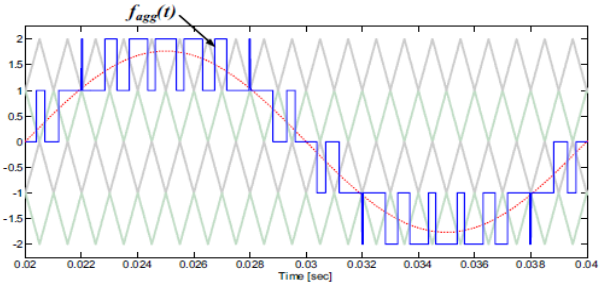

Fig.3 carrier signal waveform of alternative phase opposition disposition

(2)Phase disposition (PD) : - In phase disposition the carrier signals are in phase.

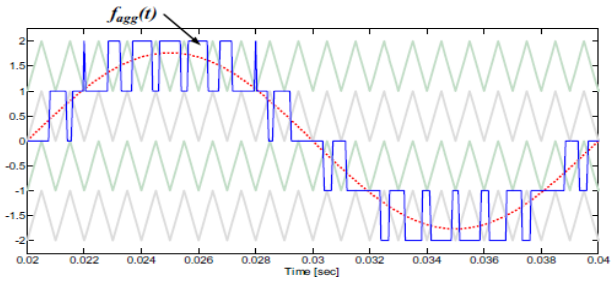

Fig. 4 Carrier signal wave of phase disposition

(3)Phase opposition disposition (POD) - in POD the carrier signals are all in phase above and below the zero reference but phase difference of 180°.

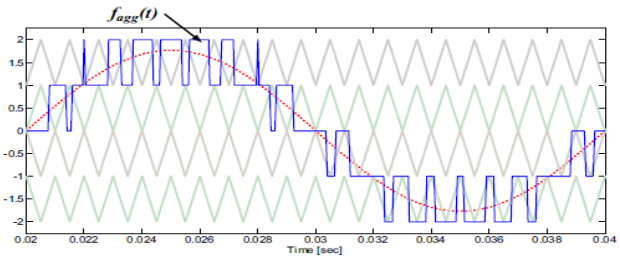

Fig.5 carrier signal wave of phase opposition disposition

Phase shifted PWM –

In phase shifted PWM carrier signals have same amplitude and all are phase shifted.

Hybrid H-

The hybrid is the combination of phase shifted and level shifted technique.

Sinusoidal pulse width modulation (SPWM):- The SPWM technique provides the way for pushing the predominant harmonics to a high frequency. In SPWM technique the comparison between the carrier signal of high frequency and modulating signal of the desired frequency can be easily done. Increasing the switching frequency leads to deduction in lower order harmonics from the output Voltage.

$V_m = m \sin(\omega + j\, 2\pi/3)$ ---------- (6)

$m = A_m/A_{u1}+A_{u2}+A_{l1}+A_{l2}$ ---------- (7)

$m_f = f_c/f_m$ ---------- (8)

where j = 0, -1, +1 x = a, b, c,

m = modulation index, mf = frequency ratio, f_c = carrier wave frequency, f_m = modulating wave frequency, A_m = modulating wave to peak amplitude, A_{u1}, A_{u2}, A_{l1}, A_{l2} = upper1, upper2, lower1 and lower2 carrier waves peak -to-peak amplitudes.

The fig 5(b) shows three phase bridge inverter fed induction motor.

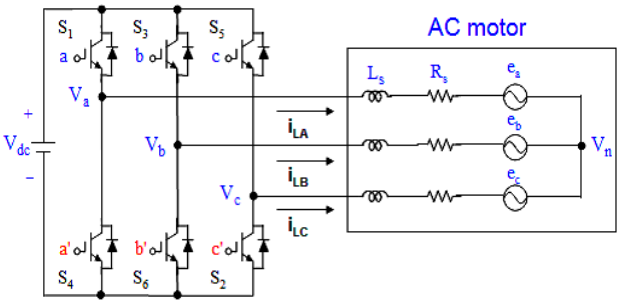

Fig.5 (b) Bridge inverter

IV. SIMULATION RESULTS

Fig. 6 show the output line to line voltage waveform of three level cascaded H-Bridge multilevel inverter.

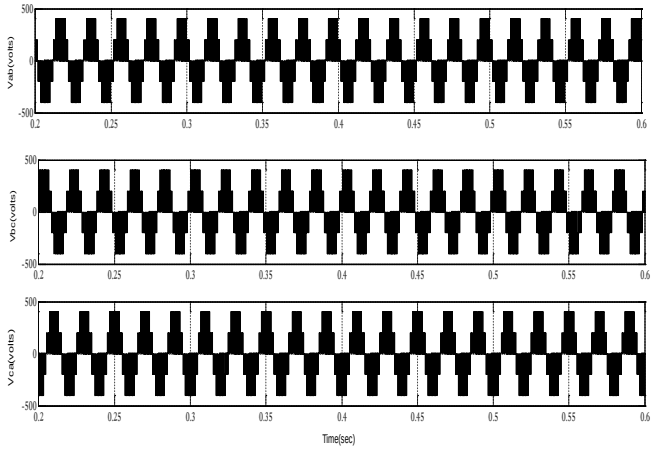

Fig.6 Three-level cascaded H-Bridge line to line voltage waveform.

Fig. 7 show the output line to line voltage waveform of five level cascaded H-Bridge multilevel inverter.

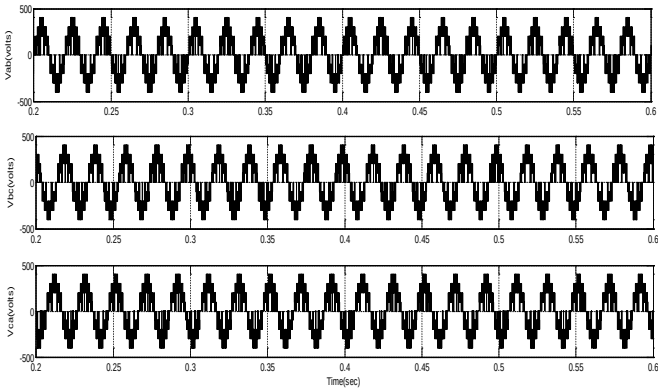

Fig.7 Five-level cascaded H-Bridge line to line voltage waveform.

Fig. 8 show the output line to line voltage waveform of seven level cascaded H-Bridge multilevel inverter.

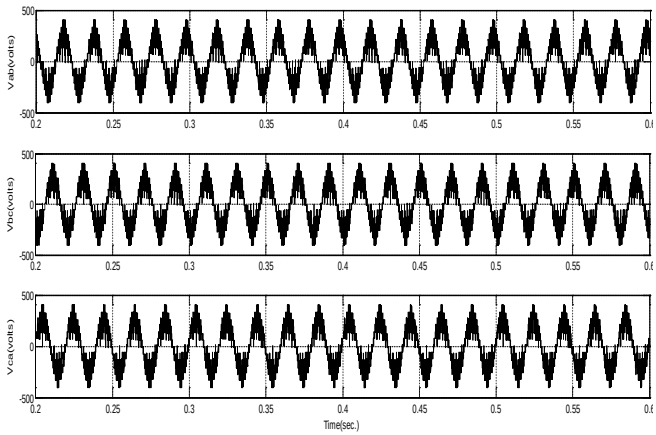

Fig.8 Seven-level cascaded H-Bridge line to line voltage waveform.

Fig. 9 show the output line to line voltage waveform of nine level cascaded H-Bridge multilevel inverter.

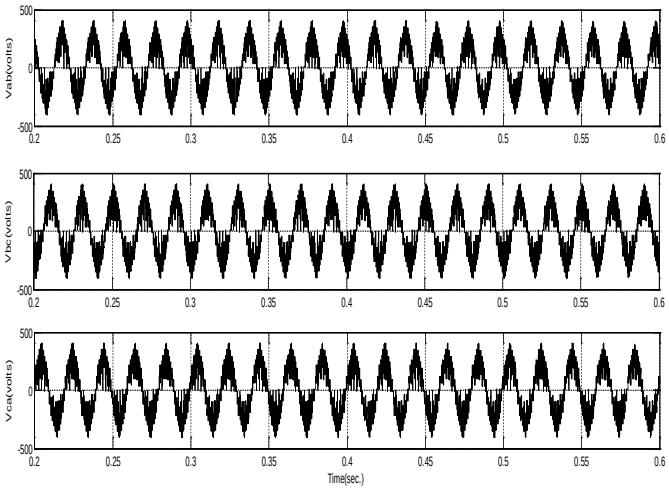

Fig.9 Nine-level cascaded H-Bridge line to line voltage waveform.

Fig.10 Show the rotor speed of induction motor fed by cascaded three level H-Bridge inverter. The speed will remain constant at 1480rpm**.**

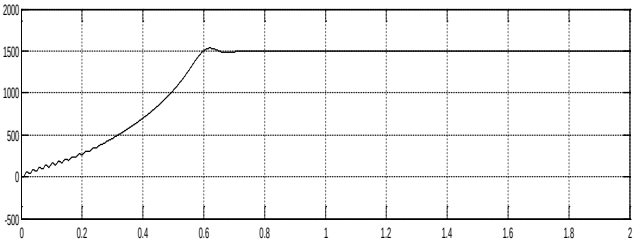

Fig10.Rotor speed of cascaded three level inverter fed induction motor

Fig.11 Show the rotor speed of induction motor fed by cascaded five-level H-Bridge inverter. The speed will remain constant at 1480rpm**.**

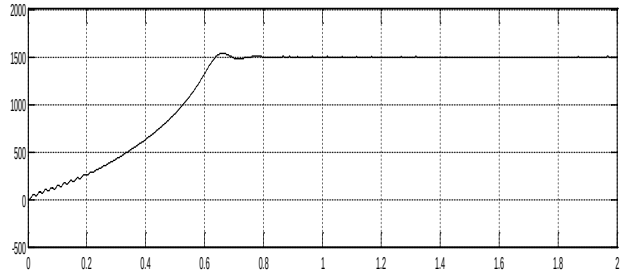

Fig11. Rotor speed of cascaded five level inverter fed induction motor.

Fig.12 Show the rotor speed of induction motor fed by cascaded seven-level H-Bridge inverter. The speed will remain constant at 1480rpm**.**

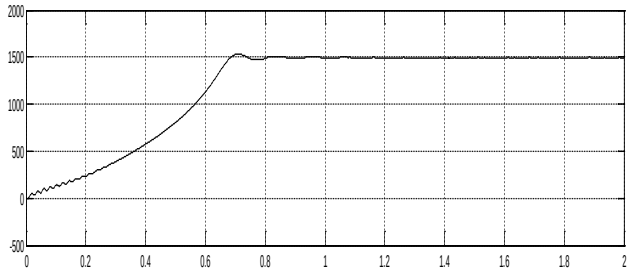

Fig.12 Rotor speed of cascaded seven level inverter fed induction motor.

Fig.13 Show the rotor speed of induction motor fed by cascaded nine level H-Bridge inverter. The speed will remain constant at 1480rpm**.**

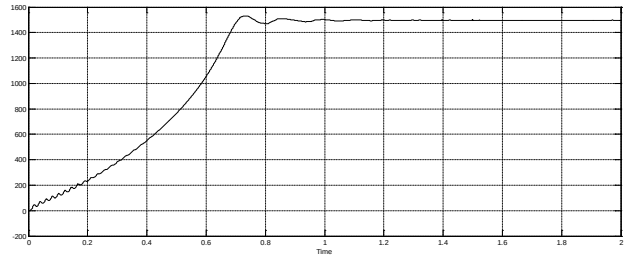

Fig.13 Rotor speed of cascaded nine level inverter fed induction motor.

Fig.14 shows the simulation model of nine-level inverter fed induction motor drives. Where I_a, I_b and I_c is the line current and V_{ab}, V_{bc}, V_{ca} is the line voltage and we analyze the performance of the motor at different level of inverter.

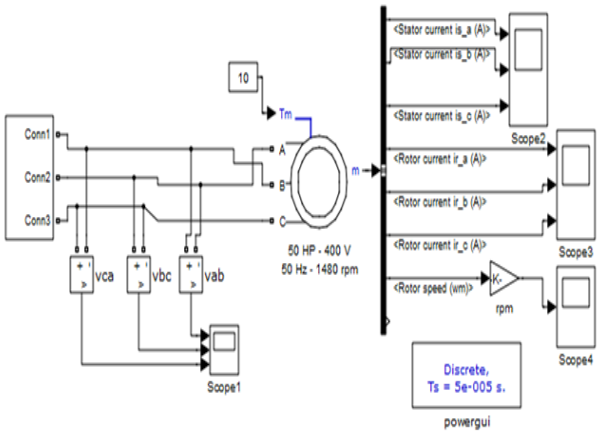

Fig.14. Nine-level inverter circuit fed induction motor simulation model.

Fig.15 shows the simulation model of cascaded nine-level inverter and the PWM circuit to generate the gating signals for the multilevel inverter switches.

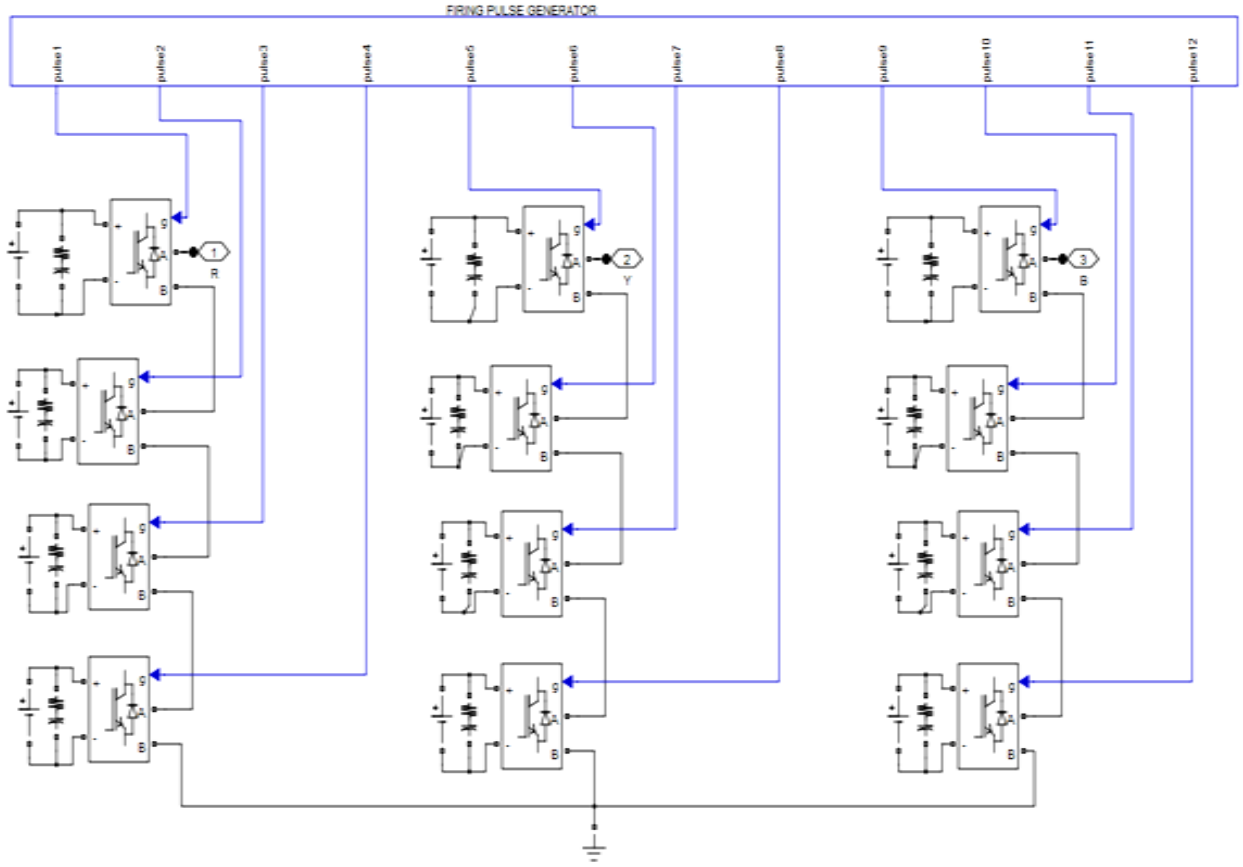

Fig.15 Simulation model of cascaded nine-level inverter.

The % total harmonic distortion of cascaded line inverter voltage is shown in table no.2

Table2.(%THD value)

Level	THD
Three level	11.06%
Five level	8.94%
Seven level	5.64%
Nine level	5.36%

V. CONCLUSION

A comparative analysis of total harmonics output line to line voltage of three-level, five-level, seven-level, and nine-level cascaded H-Bridge multilevel inverters fed with induction motor is presented in this paper. It is observed that the level of inverter increase there is an improvement in the performance of induction motor. The total harmonics distortion of line to line voltage and phase current decrease with increase in the levels of inverter.

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