An Extensive Survey of Literature on Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA

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Abstract- The design of high-speed and low-power VLSI architectures need efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption. Adders are the key components in general purpose microprocessors and digital signal processors. They also find use in many other functions such as subtraction, multiplication and division. As a result, it is very pertinent that its performance augers well for their speed performance. Furthermore, for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance. This examination presents an extensive survey of literature on Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA.

Keywords- Multiplier, Adder, Binary Multiplication, CSLA, CLAA, and Ripple Carry Adder.

I. INTRODUCTION

As the performance of processors has increased, the demand for high speed arithmetic blocks has also increased. With clock frequencies approaching 1 GHz, arithmetic blocks must keep pace with the continued demand for more computational power. The purpose of this thesis is to present methods of implementing high speed binary multiplication. In general, both the algorithms used to perform multiplication, and the actual implementation procedures are addressed. The emphasis of this thesis is on minimizing the latency, with the goal being the implementation of the fastest multiplication blocks possible.

Power dissipation is one of the most important design objectives in integrated circuit, after speed. Digital signal processing (DSP) circuits whose main building block is a Multiplier-Accumulator (MAC) unit. High speed and low power MAC unit is desirable for any DSP processor.

This is because speed and throughput rate are always the concerns of DSP system. Due to rapid growth of portable electronic systems like laptop, calculator, mobile etc., and the low power devices have become very important in today world. Low power and high-throughput circuitry design are playing the challenging role for VLSI designer. For real-time signal processing, a high speed and high throughput MAC unit is always a key to achieve a high performance digital signal processing system. A regular MAC unit consists of multipliers and accumulators that contain the sum of the previous consecutive products. The main motivation of this work is to investigate various multiplier and adder architectures which are suitable for implementing Low power, area efficient and high speed MAC unit.

Multiplication is a mathematical operation that at its simplest is an abbreviated process of adding an integer a specified number of times. A number (multiplicand) is added to itself a number of times as specified by another number (multiplier) to form a result(product). In elementary schools, students learn to multiply by placing the multiplicand on top of the multiplier. The multiplicand is then multiplied by each digit of the multiplier beginning with the rightmost, least significant digit (LSD). Intermediate results (partial-products) are placed one atop the other, offset by one digit to align digits of the same weight. The final product is determined by summation of all the partial-products. Basic multiplication technique is shown in figure 1.1:

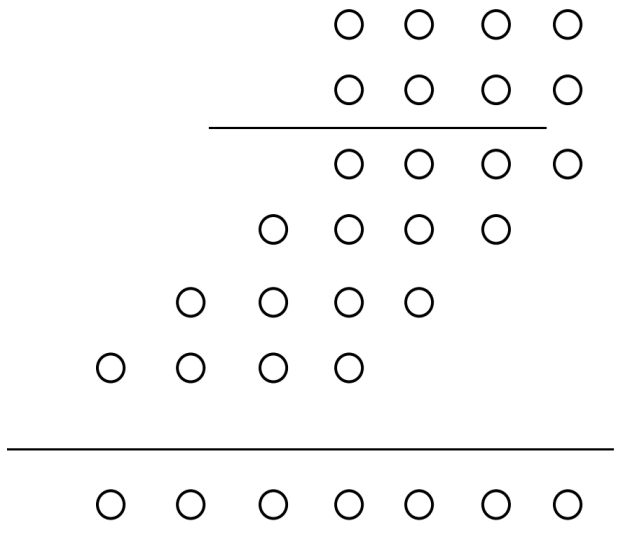


Figure: 1.1 Basic Multiplications.

In the binary number system the digits, called bits, are limited to the set [0,1]. The result of multiplying any binary number by a single binary bit is either 0, or the original number. This makes forming the intermediate partial-products simple and efficient. Summing these partial- products is the time consuming task for binary multipliers. The two main categories of binary multiplication include signed and unsigned numbers. Digit multiplication is a series of bit shifts and series of bit additions, where the two numbers, the multiplicand and the multiplier are combined into the result. Considering the bit representation of the multiplicand x= xn-1…. x1x0 and the multiplier y= yn-1….y1y0 in order to form the product up to n shifted copies of the multiplicand are to be added for unsigned multiplication. The entire process of multiplication is divided in 3 par5ts.

1) Generate the Partial Products

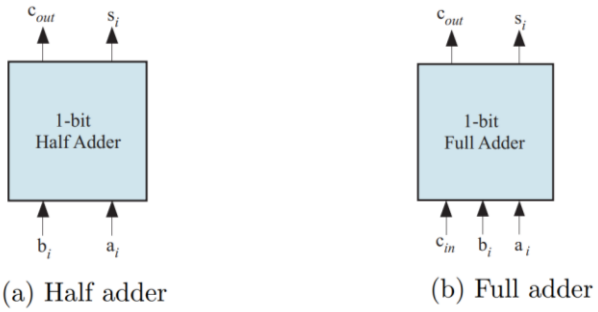
2) Partial Product Reduction.

3) Final stage Carry Propagate Adder

II. THE ADDERS

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit.

Adders are one of the key components of any data path. As any component in VLSI design, the choice of adder architecture is constrained by the important factors of area, speed and power.



(a) Half adder (b) Full adder

Fig. 2.1 Basic Adders modules.

The adder is an essential computing component that is discussed widely in digital circuit design. Various applications including a high-performance processor, embedded processors, and DSP processors rely on the adder component in order to perform algorithm operations in their arithmetic logic units (ALUs). Adders also used in other parts of the processor to calculate addresses, table indices, increment and decrement operators. Due to this reason, addition is the most frequently used operation in a digital circuit that represents the main role for the computational speed of a system.

a. Ripple Carry Adder

Ripple carry adders are one of the most simple adder architectures available. A n-bit ripple carry adder is made of up a collection of n number of individual full adder cells. These adders are simple in design and also they occupy less area. But they are constrained in their performance capabilities. For the modern day designs where high speed of operation is required, these adders fall short by a large extent as the delay through the adder chain to produce the output is very large. Hence, these adders are not very popular to be implemented in the modern day designs. Because of their simplicity in design there are certain circuit implications which can be efficiently implemented using ripple carry adders

b. Carry Look-Ahead Adders

As seen earlier ripple carry adders are limited in their performance capabilities. So, adders with improved performance are required. Carry look-ahead adders are one such solution. As the name suggests, in carry look-ahead adders the carry chain is generated ahead of time utilizing all of the inputs to improve the addition operation. This is achieved at the expense of increased area and power in the form of increased number of gates.

c. Carry Select Adders

Carry select adders are one of the other popular architectures which show improved performance over ripple carry adders. As in ripple carry adders they are popular for their regular layout structure. These adders basically consist of blocks where each block executes two additions. One assumes that the input carry is ‘1’ and the other assumes that the input carry is ‘0’. The input carry signal ‘0’ generates a block generate signal and the input carry signal ‘1’ generates a block propagate signal which are used to produce the carry out signal for the subsequent block which selects the appropriate set of sum bits.

d. Carry Save Adder

Carry save adder are based on the idea that a full adder really has three inputs and produces two outputs. While it usually associates the third input with a carry in, it could equally well be used as a regular value. The full adder can be used as 3:2 reduction networks. It takes three bits from 3 words, adds them and produces two bits, one for sum and other for carry bits wide. An n-bit carry save adder can be built by using n separate adders. The name carry save arises from the fact that save the carry out words instead of using it immediately to calculate the final sum. Carry-save

adders are useful in situations where need to add more than two numbers.

III. RELATED WORK

SR. NO.	TITLE	AUTHORS	YEAR	APPROACH
1	Design and implementation of 32 bit unsigned multiplier using CLAA and CSLA	V. Vijayalakshmi, R. Seshadri and S. Ramakrishnan,	2014	Carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier
2	Design of a Parallel Adder Circuit for a Heavy Computing Environment and the Performance Analysis of Multiplication Algorithm,"	J. K. Das, P. P. Choudhury and S. Sahoo,	2017	A new parallel adder circuit model in Carry Value Transformation (CVT)-Exclusive OR (XOR) paradigm.
3	Majority Logic Formulations for Parallel Adder Designs at Reduced Delay and Circuit Complexity,	V. Pudi, K. Sridharan and F. Lombardi,	2017	Two new majority gate-based recursive techniques are proposed. The first technique relies on a novel formulation of the majority gate-based equations. The second contribution of this manuscript utilizes recursive properties of majority gates
4	Design and performance analysis of modified unsigned braun and signed Baugh-Wooley multiplier,	V. B. Biradar, P. G. Vishwas, C. S. Chetan and B. S. Premananda	2017	Involves design and implementation of modified Baugh-
5	CLA based 32-bit signed pipelined multiplier,	S. Bokade and P. Dakhole,	2016	The proposed 32-bit multiplier is based on pipelining
6	Design of high speed multiplier using modified booth algorithm with hybrid carry look-ahead adder	R. Balakumaran and E. Prabhu	2016	A novel method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid carry look-ahead adder
7	128 Bit unsigned multiplier design and implementation using an efficient SQRT-CSLA,	M. Gopi and G. B. S. R. Naidu,	2015	The new Carry Select Adders (CSLA) to enhance the multiplier performance
8	Design of low power and high speed Carry Select Adder using Brent Kung adder	P. Saxena,	2015	Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA)

V. Vijayalakshmi, R. Seshadri and S. Ramakrishnan,[1] This project deals with the comparison of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier and the VLSI design of the carry select adder (CSLA) based 32-bit unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay time of 99ns for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31% by the CSLA based multiplier to complete the multiplication operation. These multipliers are implemented using Altera Quartus II and timing diagrams are viewed through avan waves.

J. K. Das, P. P. Choudhury and S. Sahoo,[2] Firstly, this study proposed a new parallel adder circuit model in Carry Value Transformation (CVT)-Exclusive OR (XOR) paradigm. Secondly, an efficient multiplication algorithm

is discussed along with its performance analysis on various inputs selection. Our design of proposed model for the addition of many integer pairs using parallel Cellular Automata Machines (CAMs) can perform the addition in a much better way with setting a preprocessing testing logic in it. CVT and XOR operations together can do the efficient addition of two non-negative integers for any bulk inputs using CAM. Multiplication is the repetitive addition process, which could be designed using recursive use of CAM. Our analysis up to 10 bits selection of all integer pairs suggest that the recursive use of CAM for multiplication becomes much faster in real life scenario for any types of inputs. Further exponential operation is highly needed for various fields of computer science which is also described in this paradigm.

V. Pudi, K. Sridharan and F. Lombardi,[3] The design of high-performance adders has experienced a renewed interest in the last few years; among high performance schemes, parallel prefix adders constitute an important class. They require a logarithmic number of stages and are typically realized using AND-OR logic; moreover with the emergence of new device technologies based on majority logic, new and improved adder designs are possible. However, the best existing majority gate-based prefix adder incurs a delay of 2log2(n) - 1 (due to the nth carry); this is only marginally better than a design using only AND-OR gates (the latter design has a 2log2(n) + 1 gate delay). This examination initially shows that this delay is caused by the output carry equation in majority gate-based adders that is still largely defined in terms of AND-OR gates. In this examination, two new majority gate-based recursive techniques are proposed. The first technique relies on a novel formulation of the majority gate-based equations in the used group generate and group propagate hardware; this results in a new definition for the output carry, thus reducing the delay. The second contribution of this manuscript utilizes recursive properties of majority gates (through a novel operator) to reduce the circuit complexity of prefix adder designs. Overall, the proposed techniques result in the calculation of the output carry of an n-bit adder with only a majority gate delay of log2 (n) + 1. This leads to a reduction of 40percent in delay and 30percent in circuit complexity (in terms of the number of majority gates) for multi-bit addition in comparison to the best existing designs found in the technical literature.

V. B. Biradar, P. G. Vishwas, C. S. Chetan and B. S. Premananda, [4] Adders and Multipliers play a vital role in the functioning of various systems used in communication and signal processing. Baugh Wooley and Braun multipliers employ parallel architecture and hence they are the most frequently used multipliers for signed and unsigned operations. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. This work involves design and implementation of modified Baugh-Wooley and Braun multipliers for signed and unsigned number multiplication respectively and analysis with respect to speed and power consumption of the designed multipliers. The adder is designed using three different logics, namely, Basic CMOS, Domino and Split Path Data Driven Dynamic Logic (SPD3L). The designed adder is then used to construct the multipliers. An improvement in power and reduction in delay is observed for both the designed multipliers.

S. Bokade and P. Dakhole, [5] In this examination, Radix-4 Modified Booth Encoding (MBE) is used to generate partial product. The proposed 32-bit multiplier is based on pipelining. The main target is to reduce the delay of higher bits multiplier and speeding up the computation. The proposed design is implemented in Xilinx 14.2. The delay achieved is 2.826ns for computing 32×32 bit signed multiplication with maximum frequency of 353.832 MHz on the device 7vx330tffg1157-3.

R. Balakumaran and E. Prabhu, [6] n this examination novel method for multiplier and accumulator is proposed by combining reversible logic functions and hybrid carry look-ahead adder. Modified booth algorithm produces less delay in comparison with a normal multiplication process and it also moderates the number of partial products. The Carry look-ahead adder is used for controlling the overall MAC delay. The main purpose of designing a reversible logic is to reduce the circuit complexity, power consumption and loss of information. Here survey on possible ways to make a full adder design using different reversible logic gates. Also reported a new hybrid CLA from the existing hierarchical CLA which exhibits high performance in terms of computation, power consumption and area in this examination. Area, delay and power complexities of the resulting design are reported. The proposed MAC shows better performance compare to conventional method and has advantages of reduced area overhead and critical path delay. This new high speed hybrid carry look-ahead adders are simulated and synthesized using Synopsys (90 nm) Design Compiler and Xilinx ISE simulator.

M. Gopi and G. B. S. R. Naidu [7] In Digital systems like digital signal processors, FIR filters and micro processors etc, Multiplier is one of the main hardware blocks. Generally, the performance of system is determined by the multiplier performance because the multiplier is generally the slowest element in the whole system and also it is occupying more area. In the multiplier, use adder circuit repeatedly. So, an efficient adder circuit will be used in multipliers, it gives better performance. In the proposed work placing the new Carry Select Adders (CSLA) to enhance the multiplier performance. Carry Select Adder

(CSLA) provides better performance with respect to speed and area. Previously a binary to excess one converter (BEC) based Square Root Carry Select Adder is designed but in that data dependency is very high, it gives some speed penalty. An efficient CSLA design is obtained using improved logic units to eradicate the data dependency and redundant logic operations. In this proposed work, the intended efficient Square Root Carry Select Adder is compared with BEC based CSLA of respective architectures, after having comparison the proposed CSLA is efficient with respective to area and delay is used in Multiplier design. This work gives better results regarding to the performance parameters such as delay and area of designed multiplier using new efficient square root carry select adder compared to BEC based CSLA multiplier.

P. Saxena, [8] In this examination, Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore have replaced it with parallel prefix adder which gives fast results. In this examination, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. Power and delay of all these adder architectures are calculated at different input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of power but with small speed penalty. The designs have been synthesized at 45nm technology using Tanner EDA tool.

IV. PROBLEM STATEMENT

Multiplication is the key in arithmetic operation and multiplier plays an important role in digital signal processing. Unfortunately, the major source of power dissipation in digital signal processors is multipliers. In the past decade, researchers developed multipliers with the help of CMOS logic, which has all the disadvantages as discussed earlier. Therefore, the design of multipliers for digital signal processing applications should be efficient while still being able to handle low-power applications. So, there is a need to design a fast multiplier, which shows improvements over CMOS designs. Several case studies show that pass logic principle based design implements most functions with fewer transistors which reduces the overall capacitance than static CMOS; thus, resulting in faster switching times and lower power. In ASIC design the performance of multiplier can be improved by utilizing a desired Adder architecture.

V. CONCLUSION

Multiplication is a frequently utilized operation in much application especially in signal processing applications. So the design of multiplier architecture is vital for applications in portable mobile devices like personal multimedia players, cellular phones, digital cam coders and digital cameras etc. This examination reviewed concept of binary multiplication and various multiplier architecture proposed recently in literature. Though being an essential block multiplier has some limitation of speed power and area which is directly impact on performance of device or application multiplier used. The problems of designing and implementation of multiplier are discussed under problem statement section. This examination reported Survey of literature on design and implementation of multiplier which led to design an efficient multiplier in future.

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