Design of a Low Power Low Drop Out Linear Voltage Regulator using 0.6µm Technology

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Abstract: ***This paper focuses on the design of a very low power low dropout linear voltage regulator (LDO) IC with reduced feature size. Not only lead to the reduction of the required PCB space and component cost, but also make the power management more efficient and reasonable. In order to improve efficiency, the PMOS transistor is adopted to achieve the low dropout voltage. The bypass circuit is designed to reduce the output voltage noise and improve power supply rejection, which make the chip adapt to audio devices. Furthermore, its fast start-up circuit is designed to reduce the start-up time. The circuit is added to ensure the stability in whole load range, improve the transient response and greatly reduce the cost of the application.***

Keywords: LDO (Low Drop Out voltage regulator), NMOS, FOM (Figure of Merit).

I. INTRODUCTION

Voltage Regulator basically regulates the voltage value in a specific range. There are two basic types of linear regulator. One is the series regulator and the other is the shunt regulator. A series or low dropout linear regulator (LDO) is a circuit that supplies a good specified and stable DC voltage [2]. In summary, linear regulators can be high or low power, externally or internally compensated, and high or low dropout, as depicted in Fig.1-2 [3].

The presented paper focuses on low dropout (LDO) linear voltage regulators. LDOs provide a constant voltage supply and are a very important part of a power management system. At input voltages close to the output voltage, the LDO regulator is much more efficient over conventional linear regulators. In addition to efficiency improvements, LDOs have more advantages over linear regulators making them more suitable for SoC power management solutions.

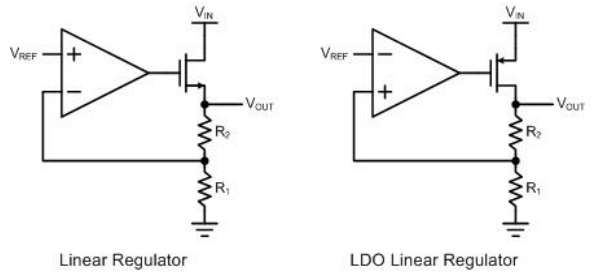


Figure 1: Conventional and LDO Linear Regulator Topologies Both of the linear regulator topologies use the same feedback

II. RELATED WORK

Load Conditions: The regulator to be designed should have good DC regulation characteristics but the main purpose for the LDO is the ability to supply power for digital control circuitry. Estimated complexity for the digital load is roughly 100000 equivalent gates. For simulation purposes the load circuit was modeled with DFFs and inverters clocked simultaneously with a 5MHz clock. In addition, measurement data from a similar, implemented load revealed that the maximum average current drawn by the digital load is 1-3mA. Table 2 provides the approximated characteristics of the pulsed load current based on the simulations and measurement data.

Table 2. Characteristics of the pulsed load current

Max. peak current	90Ma
Frequency	5MHz
Rise & fall time	2ns
Pulse width	5ns

Evidently, the load current pulses are outside the bandwidth of the LDO which implies that the filtering of the output voltage relies on the output capacitor. The maximum allowable voltage drop from a single current pulse was defined to be 100 mV. The theoretical value for the output capacitor can be calculated. Considering the load specifications in Table 2, the minimum output capacitance should be 6.3nF, which obviously is too large to be integrated on silicon. This implies that an external capacitor is necessary for highly dynamic pulsed loads; e.g. if the output voltage filtering relied on an integrated 100pF capacitor, the voltage drop due to a maximum current pulse would be intense, resulting in an undershoot close to the ground potential. For the reasons mentioned above, two LDOs will be designed: an integrated one for driving on-chip analog blocks utilizing a 100pF output capacitor and an LDO with an external capacitor for driving the digital load described in Table 2.

In order to determine the practical value for the external capacitor, the voltage drop induced by a full range load current step was simulated with different output

capacitance values. Figure 24 illustrates the magnitude of the voltage drop with different maximum peak current values.

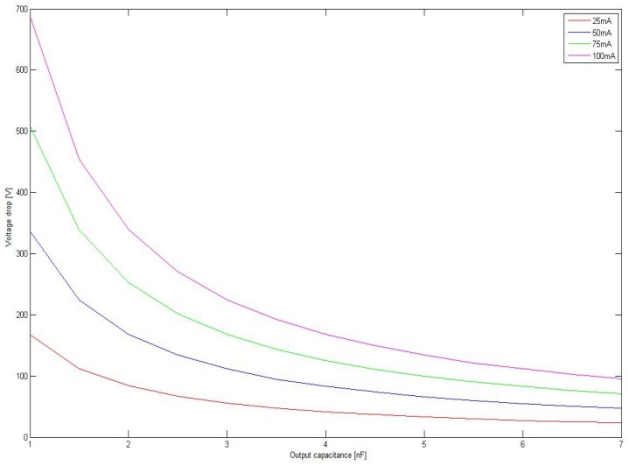
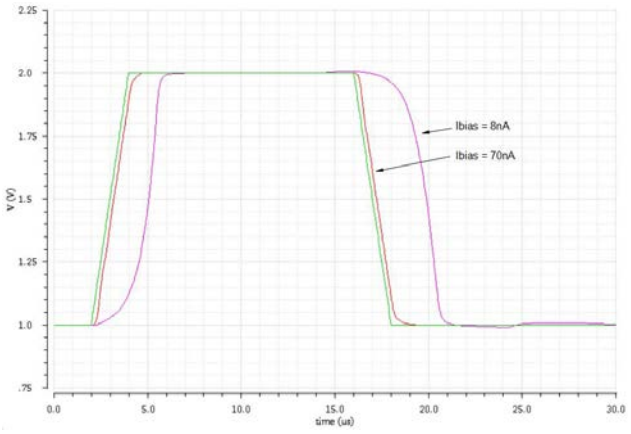


Figure 4.1. The voltage drop induced by a pulsed load current step as a function of output capacitance.

Based on the simulation results, a 7nF external capacitor will be used in order to provide sufficient filtering when the logic load is enabled.

The Error Amplifier: The final design utilizes the class AB OTA with the improved FVF circuits as the error amplifier due to its superior performance in low power environments.The most important design parameter for the amplifier is the static power consumption. To achieve the minimum quiescent current consumption of 100nA, the bias current should be roughly 8nA during standby. Although such a bias point is possible without significant degeneration in slew rate, the small current does however increase the impedance levels inside the amplifier which essentially causes delay.



To minimize this, 10fF capacitors C2 and C3 were added into the FVF feedback loop in order to increase the speed of the amplifier in low current conditions. The delay occurs only in the low biasing points; even a slight increase in the quiescent current improves the dynamic performance significantly. The inevitable consequence of the low bias is the delay which is approximately 2μs on the rising edge and 3 μs on the falling edge. However, when the bias current is slightly increased, the amplifier response improves significantly.

Adaptive Biasing: The current sensing circuitry presented in Section 3.4 is used to generate a bias voltage equivalent to the load current. Figure 26 illustrates the final design of the adaptive biasing circuit.

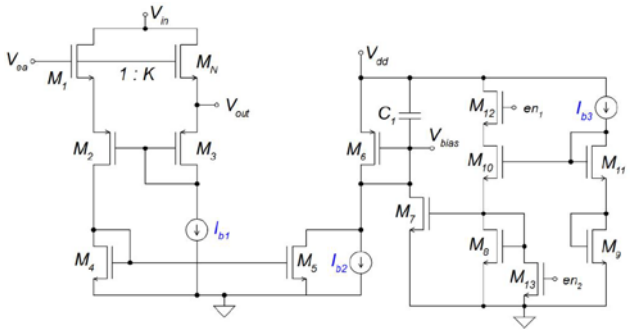
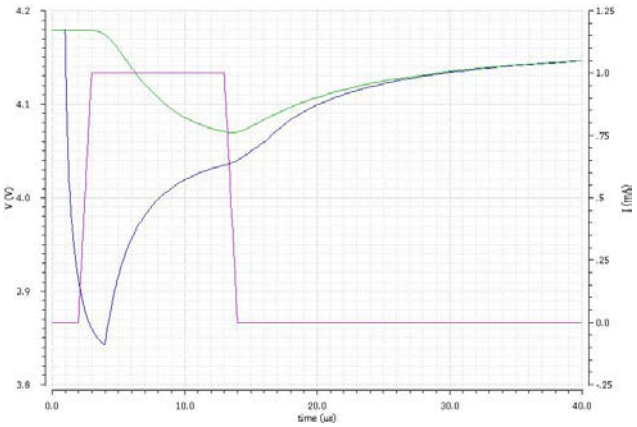


Figure 4.4. The complete adaptive biasing circuit.

The extra circuitry consisting of transistors M7-M13 form a booster circuit, the purpose of which is to quickly sink current through M6 and therefore increase the bias of the amplifier when the actual adaptive bias circuit is unable to react fast enough. The functionality of the booster is controlled by transistors M12 and M13. During normal operation, the gate of M7 should be grounded by enabling en2. The booster is activated by enabling en1 and disabling en2 which causes M7 to sink a constant current. As en1 is disabled, the voltage at the gate of M7 discharges gradually resulting to a soft transition to the actual bias voltage level. After the voltage settles to a desired level, en2 opens M13, pulling the gate of M7 firmly to ground.

The effect of the booster circuit on the reaction speed is illustrated in Figure below which presents how output voltage of the biasing circuit reacts to a change in the load current.



The booster circuit not only allows the amplifier to be biased faster, but also to a higher bias point during startup which results in improved response to the load step in terms of undershoot and settling time.

The output voltage bias circuitry has to be limited though, as the maximum DC output current is designed to be 100mA. If the bias voltage drops too low due to the high load current, it will decrease the voltage levels inside the error amplifier and eventually decreases performance. In addition, the bias point affects to the position of the dominant pole; if the amplifier is biased too high, the position of the dominant approaches the output pole, decreasing phase margin. Hence, the bias circuit is adjusted so that the lowest bias voltage for the amplifier will be roughly 3.6V.

The Charge Pump: The primary requirement for the charge pump is the ability to supply a sufficient amount of current, because the operational amplifier requires large amounts of current during heavy transients. To ensure that the output voltage of the charge pump will not undershoot too low, it should be able to supply roughly 50µA of current. The output resistance should be kept as low as possible to minimize the voltage drop when current is drawn from the charge pump. To minimize the output resistance, the circuit will utilize two phases; this configuration essentially halves the output resistance and also allows smaller capacitors to be used. The circuit is clocked with non-overlapping, 10MHz clock signals. Figure 4.14 illustrates the startup of the charge pump after it is enabled.

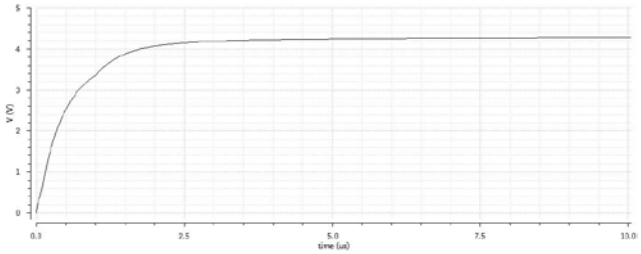


Figure 4.14. Charge pump startup

The Final LDO Model: The top level schematic of the circuit elements in the LDO is presented in Figure 4.15. All components, including the passive ones, were modelled using components from the 0.6µm CMOS process.

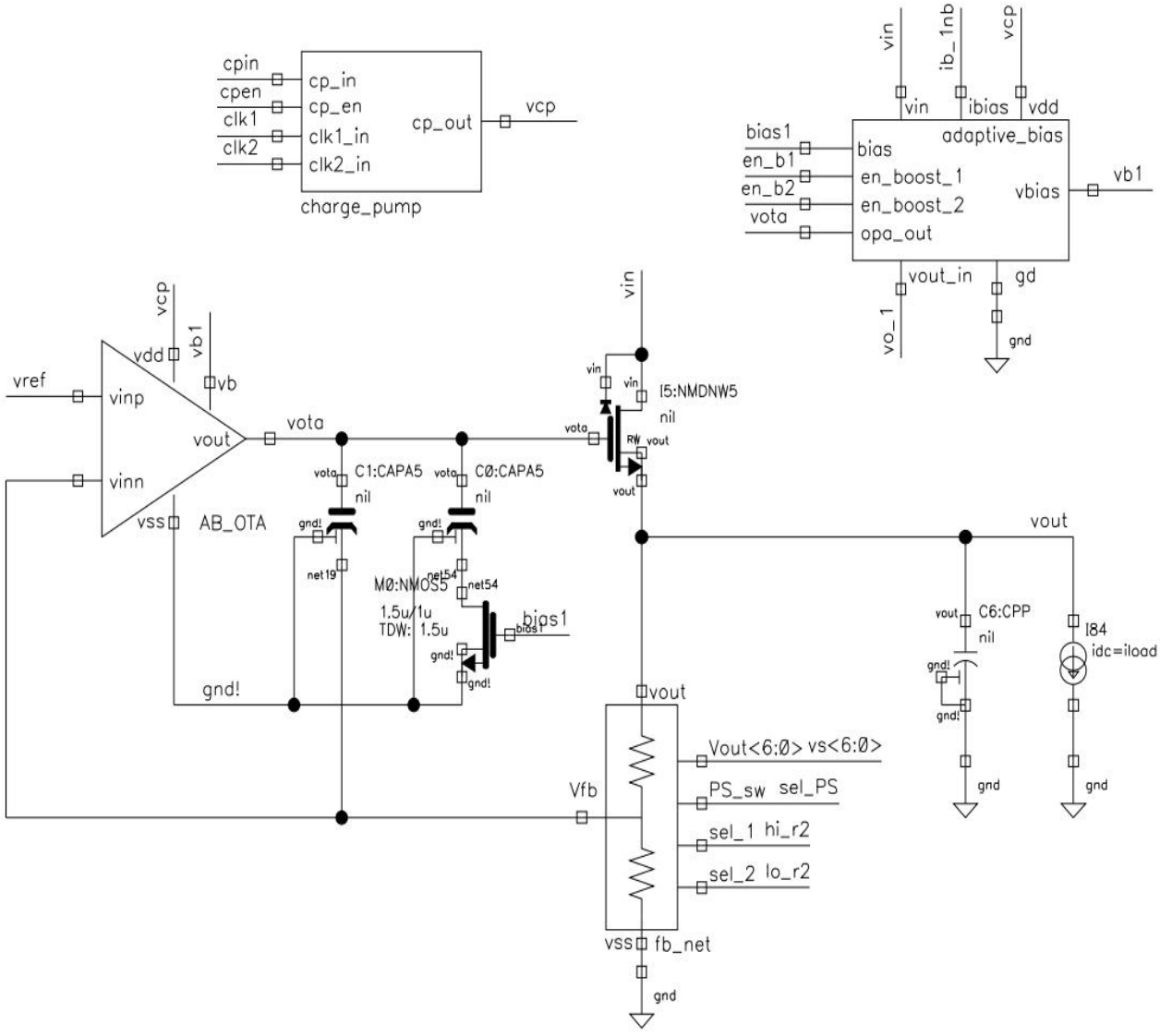


Figure 4.15 . Top level schematic of the designed LDO.

III. EXPERIMENTAL RESULTS

Below is the schematic used for bench evaluation.

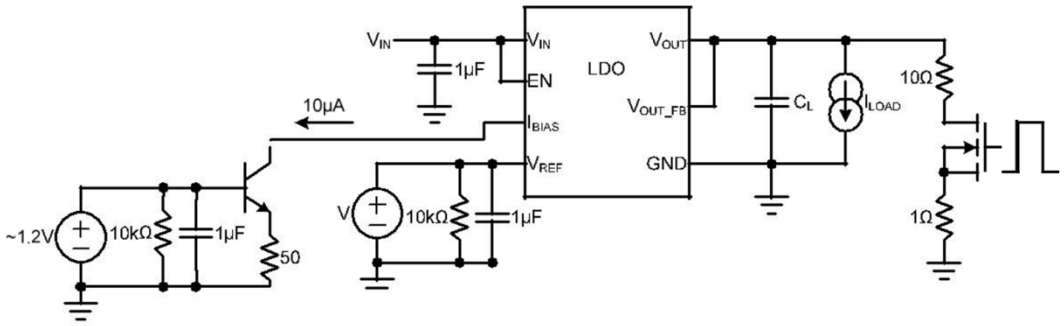
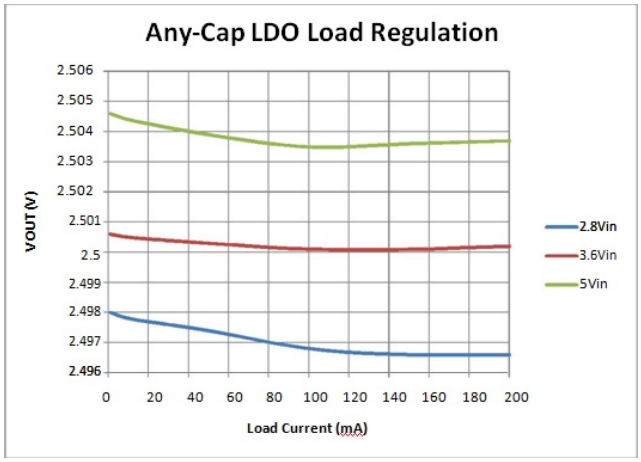


Figure 5.1: Lab Bench Evaluation Schematic

The external NMOS with 10Ω in the drain and 1Ω in the source is used for the load step evaluation. The 1Ω source degeneration resistor is an accurate current sense resistor so that a voltage probe can be placed across it to look at the load step current with a scale of 1A/V. The gate voltage of the NMOS can be varied to give a desired load step current less than 227mA.

At first power up, the LDO output regulates to ~2.5V with a 1.25V reference voltage. The minimum load current for stability is <1mA, but 1mA will be used for the minimum load. The input current with a 1mA load is 1.2mA meaning that the chip is consuming 200µA.

Load Regulation: Load regulation is measured by sweeping the load current from minimum to maximum load and the input voltage can be stepped as well. In this case, the load current was swept from 1mA to 200mA while stepping the input voltage at 2.8V, 3.6V, and 5V. Below is the load regulation plot.



The load regulations measured at -7.03mV/A, -2.01mV/A, and - 4.51mV/A at 2.8V, 3.6V, and 5V respectively. These numbers aren't exactly what the simulator predicted, but they're close enough.

The FOM was calculated for the designed integrated LDO interpreting TS as the settling time within 5% of the nominal output voltage. The settling time was measured from the LDOs response to a load transient ranging from 8µA to 100mA. Table 1 presents the FOM in comparison to other designs.

Table 1 FOM comparison.

	[13]	[16]	This work
FOM [ns]	0.0324	0.067	0.0923

The slightly larger FOM is essentially caused by the time constant created by the compensation capacitor and the feedback resistors which increase the settling time. However, considering the strict requirements for the regulator, the designed LDO has a highly comparable FOM against the designs in Table 1.

Performance Summary:

Design/Parameters	**2010**	**2011**	**2011**	**2012**	**This Work 2017**
Technology (CMOS)	0.5µm	0.18µm	0.35 µm	90 nm	45 nm
***VDD /VOUT* (V)**	1.4/1.21	2.1/1.8	3.3/3	1/0.85	0.9/0.78
R_{ESR} **(Ω)**	na	na	na	1	1
Maximum *IQ* (*µ*A)	45	150	350	60	32
Maximum *IOUT* (mA)	100	150	100	100	100
Current efficiency (%)	99.83	99.9	99.65	99.94	99.98
Area (mm2)	0.263	0.104	na	0.0041	0.0038
FOM	0.054	0.38	5.25	0.144	0.0923
Load regulation (mV/mA) 0.17	0.12	0.38	1.5	0.28	0.23

IV. CONCLUSION

A novel LDO design has been presented that allows a wide range of output capacitors to be used. This allows the LDO to be used as a system-on-chip LDO with highly current efficient RC filter. A thorough discussion was given in chapter 4 as to how this LDO was designed.

This paper presented an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 0.9 V, fast transient response, low *IQ*, and high PSR under a wide range of operating conditions. The experimental results verified the feasibility of the proposed LDO regulator.

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