Emerging 3 Dimensional Integrated Circuits

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Abstract *- Three Dimensional(3D) Integrated Circuits utilize stacked silicon interconnect (SSI) technology, it works beyond Moore's Law to achieve higher transistors count, increased functionality and superior performance to satisfy the most demanding design requirements. Modern Soc's demands low power, less die size and high performance. This technology allows heterogeneous integration of many components such as Processor, FPGA, CPU, Memory etc. on stacked chips enabling faster computing and reduced latency. Currently 3D IC's are developing using 14nm technology in future it reaches to 5nm by 2020. Heterogeneous 3D ICs has highest logic density, bandwidth, system integration, performance on-chip resources and capability. 3D IC technology and their applications on 3D FPGAs making more sense in semiconductor industry. 3D chips are needed in mobile applications and in tablets. It has been facing more technical challenges and design complexity.*

Keywords: SSI, SoC, SiP's, FPGA, TSV.

I. INTRODUCTION

Nowadays 3D IC is a trend in the field of microelectronics for developing IC technology. 3D heterogeneous integration is independent of feature size and good for mass production. 3D IC is different from 3D system in package. Technically it is difficult to implement one transistor on the top of another transistor nothing but logic on logic because different leakage current, diffusion and ion implantation. In 2D IC all system components like memory, I/O, CPU etc are embedded in single chip so called System on Chip (SoC).

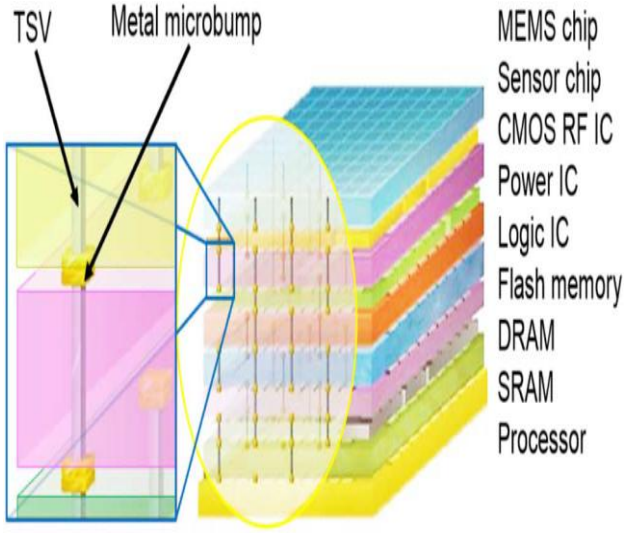

Fig 1: Overview of 3D Integrated Circuits

2D planar IC system performance is less compare to 3D IC, each component in a chip requires different power and NAND logic affects yield at some level. Interconnects between memory and CPU needed more wire bonding so it limits system performance. In 3D IC System components will be stacked on one another as shown in figure1. Bit rate depend on length of the interconnects it is reduced in mm scale. All stacks are inter connect by through silicon via (TSV) using bond wires and bumps or solder balls as shown in fig 1. Design flow of 3D circuits are unique and a variety of floor planning and routing techniques used. These circuits were very high density needs heat sink and conventional cooling effect.

II. PROPOSED METHODOLOGY

A chip in three-dimensional integrated circuit (3D-IC) technology is consists of two or more layers of active electronic components stacked, integrated vertically through silicon via. To provide vertical interconnection within each chip by drilling holes using two methods either laser ablation or deep reactive ion etching. Sides of the holes are coated with an insulator. This electrical interconnections is done by conventional c4 bumps or thermo compression bonds to reduce the inter chip spacing. 3D IC has very well electrical inter connect and mechanical stability, reliability and thermal protection. Multiple active devices are stacked side by side on an active or passive interposer. Interposer is an electrical interface routing between one another for communication. Interposer helps in maximizing the performance of the system. Bottom substrate includes batteries and power. Technology demands increasing functionality, decreasing power, to get mobility and product miniaturization. 3D IC technology gives excellent platform for achieving superior bandwidth at much lower power. Three-dimensional (3D) ICs using TSVs are high performance and low power since they have many advantages such as less cost, high speed, short wiring length, small chip size, and small pin capacitances. Several types of 3D-ICs like image sensor chip and shared memory have been fabricated successfully.

Fig 2 shows Dies with different functions, fabricated with different Technologies are integrated. To increase the speed of 3D devices clock is distributed evenly. Compare to2D, 3D is 10times faster than off- chip memory. It enables scaling limitations and 3D integration offers significant opportunities for designing highly diverse and complex systems.

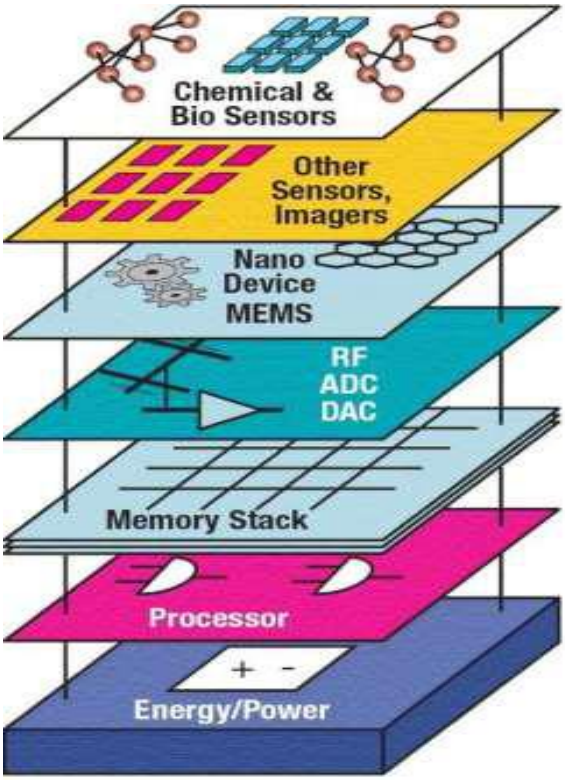

Fig 2: Heterogeneous Integration

Power/ground pads are located along the edges of the plane, providing sufficient current while satisfying target voltage levels for every transistor within IC. 3D IC is required to achieve improvements like reduced interconnect delays at higher clock rates, high bandwidth, lower power dissipation, merging different technologies and oxide, metallization for contacts.

Important considerations for the development of commercial 3D integrated systems.

- It is cheaper than 2D IC because more die per wafer with less mask steps.
- Yield increased means more number of good chips in a wafer due to small die size.
- It is technically feasible and works at low temperature below 400º C.
- Manufacturing is simple and saves more than 5 mask steps.
- It is low power up to 75% reduction of power consumption.

III. TSV TECHNOLOGY

TSV is one of key enabler and unique process to design 3D device technology through silicon via. Within the stacking of chips silicon vias gives communication link to the above and below chips and also to Vcc and Ground. Main aim of TSV is to establish good electrical connectivity between components in different dies or wafers in 3D stack.

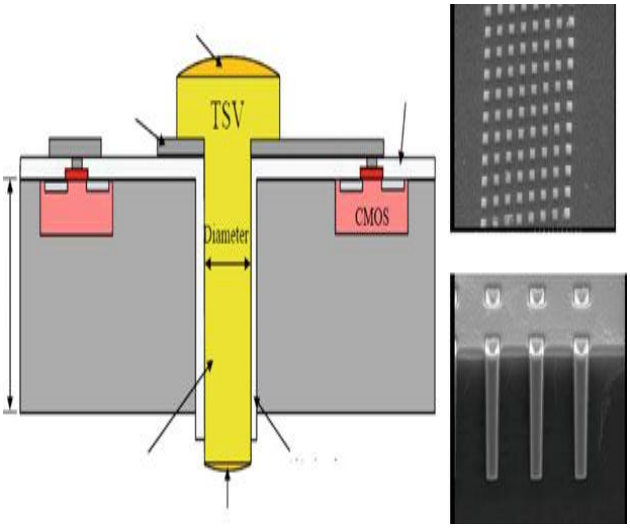

Figure 3: Through silicon via (TSV)

The TSV is better for both wafer-to-wafer and die to die stacking for high bandwidth vertical connections. First step is etching silicon material which is of length 100-150µm and center width is around 1-5µm. If width increase efficiency will decreases. It has feature of high aspect ratio and profile is uniformly vertical. Smooth and vertical TSV sidewalls after applying thick oxide layer over silicon. This oxide layer acts as insulator at high temperature. After this barrier layer is grown by diffusion process. Then metal is deposit on empty area and plating is done by using tungsten. It avoids stress and minimized. Final stage is chemical mechanical polishing to polish the outer layer and get smooth surface. Depending on the fabrication process TSV has two major types: via- first, via-middle, via-last. Thinning technology and fine pitch vertical connections plays major role for efficient power delivery and signal interconnections and thermal cooling.

IV. MERITS

- Use of buffers in 3D circuits to break up long interconnects.
- 10X faster in speed and 75% less power consumption, less space.
- Cheaper because reduced mask steps.
- Repeaters can be placed on the second layer and reduce area for the first layer.

V. DEMERITS

3D heterogeneous integration provides more benefits and it is higher density device so design complexity is there. For testing requires more CAD tools is one of the challenge in 3D circuits. Fault diagnosis and TSV repair.

VI. APPLICATIONS

1) CMOS image sensors, Microprocessor design, Mixed signal IC's

2) Power and analog components: MOSFET, IGBT, DC-DC converters

3) Logic Memory modules: DRAM, DSP, FPGA, ASIC'S, SRAM

4) Wireless SiP (System in Package): WLAN, Bluetooth, UWB

VII. CONCLUSION

3D IC is most superior performance computing including IoT. In this paper describes about the development of 3D integration and its benefits. 3D IC devices assembling very much sensitive and material selection plays main role on efficiency. Some reliability issues and thermo mechanical stress related topics still research is going on. 3D IC is successfully fabricated and many manufacturers still need EDA applications for automated design.

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Prathibha S R working has Assistant Professor at **Sambhram Institute of Technology**, Bengaluru. Completed M.tech in VLSI Design and Embedded systems and received Bachelor of Engineering degree in Electronics and communication Engineering from Channabasaveshwara Institute of Technology, Tumkur in the year 2010. Area of interest Wireless communication, Satellite communication, IoT, VLSI design, Network analysis.