Extensive Survey on Fault Tolerant Parallel FFTs with Error Correction Codes

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Abstract: Communication Engineering is been the vital field of engineering in last few decades Evolution of digital communication has made this field more interesting as well as challenging. Error correction code (ECC) techniques have been widely used to correct transient errors and improve the reliability of memories. ECC words in memories consist of data bits and additional check bits because the ECCs used in memories are typically from a class of linear block codes. During the write operations of memories, data bits are written in data bit arrays, and check bits are concurrently produced using the data bits and stored in check bit arrays. The check bit arrays, just like the data bit arrays, should be tested prudently for the same fault models if reliable error correction is to be insuredIn this paper, we study the problem of designing fault-tolerant parallel linear filters. We assume that a linear filter can either function perfectly or fail completely, i.e., generate arbitrary outputs. We use real-number error correcting codes based on linear programming decoding to introduce redundancy into the linear filters and detect faulty filters. We prove that all faulty filters can be detected and corrected if the number of faulty filters is smaller than a threshold value. We also obtain simulation results to support our statement. To the best of our knowledge, we believe that this work is the first to connect the information-theoretic idea of real-number error control coding with parallel linear filtering systems.

Keywords - ECC, Fault Tolerant Filters. FPGA.

I. INTRODUCTION

Generally communication is understood as transmission and reception of data from one place to other at some distance. In any system application we come across errors either in communication or in storage. Errors in transmission are mainly because of noise, electromagnetic interferences, cross talk, bandwidth limitation, etc. In case of storage, errors may occur because of increase in magnetic flux as in case of magnetic disc or it can be spurious change of bits because of electromagnetic interferences as in case of DRAM. The FFTs in parallel increases the scope of applying error correction codes together. Generating parity together for parallel FFTs also helps in minimizing the complexity in some ECC . By assuming that there can only be a single error on the system in the case of radiation-induced soft errors and may be two in worst case. The proposed new technique is based on the combination of Partial Summation combined with parity FFT for multiple error correction. Hence dealing with these errors when they occur is the matter of concern.

In addition, the area and timing overheads for encoder and decoder of the SEC-DED-DAEC codes are similar to those of the SEC-DED codes. Consequently, adjacent double bit errors can be remedied with very little additional cost using the SECDED-DAEC codes. The SEC-DED-DAEC codes may be an attractive alternative to bit interleaving in providing greater flexibility for optimizing the memory layout. Furthermore, the SEC-DED-DAEC code can be used in conjunction with bit interleaving and this method can efficiently deal with adjacent multi-bit errors.

The FFTs in parallel increases the scope of applying error correction codes together. Generating parity together for parallel FFTs also helps in minimizing the complexity in some ECC . By assuming that there can only be a single error on the system in the case of radiation-induced soft errors and may be two in worst case. The proposed new technique is based on the

Fast Fourier Transform: Fast Fourier Transform (FFT) algorithm converts a signal from time domain into a sequence in the frequency domain . Fast Fourier transforms are widely used for many applications which include engineering, science, and mathematics. It computes transformations through DFT matrix. The FFT operation starts with decomposing N-point time domain signal and calculating N frequency spectra and finally forming a single spectrum.

Errors and methods:

- *Automatic repeat request (ARQ) :* In this approach, the receiver first detects the error and then sends a signal to the transmitter to retransmit the signal. This can be done in two ways:

(i) continuous transmission mode

(ii) wait for acknowledgement.

In continuous transmission mode, the data is being sent by the transmitter continuously. Whenever receiver finds any error it sends a request for retransmission. However, the retransmission can either be selective repeat or go back N step type. As the name suggests, in selective repeat those data units containing error are only retransmitted. While in go back N type, retransmission of last N data unit occurs. Next, in wait for acknowledgement mode, acknowledgement is sent by the receiver after it correctly receives each message. Hence, when not sent, the retransmission is initiated by the transmitter.

- *Forward error correction (FEC):* In this approach, error is both detected and corrected at the receiver end. To enable the receiver to detect and correct the data, some redundant information is sent with the actual information by the transmitter. After being introduced to both the approaches, one should choose whether which approach is to be used. Automatic repeat request is easier but if the error occurs much frequently, then retransmission at that frequency will particularly reduce the effective rate of data transmission. However, in some cases retransmission may not be feasible to us. In those cases, Forward Error correction would be more suitable. As Forward Error Correction involves additional information during transmission along with the actual data. It also reduces the effective data rate which is independent of rate of error. Hence, if error occurs less frequently then Automatic request approach is followed keeping in mind that retransmission is feasible. Out of the various FEC's, Reed Solomon code is one. These are block error correcting codes with wide range of applications in the field of digital communications. These codes are used to correct errors in devices such as CD's, DVD,s etc.., wireless communications, many digital subscriber lines such as ADSL,HDSL etc… They describe a systematic way of building codes that can detect and correct multiple errors. In a block code we have k individual information bits, r individual parity bits and a total of n (=k+r) bits. However, reed Solomon codes are organized in group of bits. This group of bits are referred to as symbols. So we can say, this code has n number of symbols. Each symbol comprises of m number of bits, where n(max)=2^m-1

II. BASICS OF COMMUNICATION AND CODING THEORY

Communication is the phenomenon of transmitting information. This transmission can either be made between two distinct places (for ex, a phone call) or between two points in time, for example the writing of this thesis so that it can be read later on. We shall restrict ourselves to the study of digital communication. That is, the transmission of messages that are sequences of symbols taken from a set called alphabet. Digital communication has become predominant in today's world. It ranges from internet, storage disks, satellite communication to digital television and so on. Moreover, any analog system can be transformed into digital data by various sampling and signal transformation methods. Typical examples include encoding music in an mp3, numerical cameras, voice recognition and many others

- The information source outputs the data to be communicated. It produces messages to be transmitted to the receiving destination. When it is a digital source, these messages are sequences of symbols taken from a finite alphabet.
- The transmitter takes the source data as input and produces an associated signal suited for the channel. Transmitter aims to achieve one or more of the followings.
  - ➢ A maximum of information transmission per unit of time. This is directly connected to data compression techniques taking advantage of the statistical structure of the data.
  - ➢ To ensure a reliable transmission across the noisy channel. In other words, to make it fault tolerant to errors introduced by the channel. This is typically done by adding structured redundancy in the message.
  - ➢ To provide message confidentiality. This typically involves encryption which¬ hides or scrambles the message so that unintended listeners cannot discern the real information content from the message.
- The physical channel is the medium used to transmit the signal from the source to the destination. Examples of channels conveying information is conveyed over space like telephone lines, fiber-optic lines, microwave radio channels. . . Information can also be conveyed between two distinct times like for example by writing data on a computer disk or a DVD and retrieving it later. As the signal propagates through the channel, or on its storage place, it may be corrupted. For example, the telephone lines suffer from parasitic currents, waves are subject to interference issues, a DVD can be scratched... But these perturbations are regrouped under the term of noise. The more noise, the more the signal is altered and the more it is di-cult to retrieve the information originally sent. Of course, there are many other reasons for errors like timing jitter, attenuation due to propagation, carrier offset... But all these perturbations lie beyond the scope of this work.

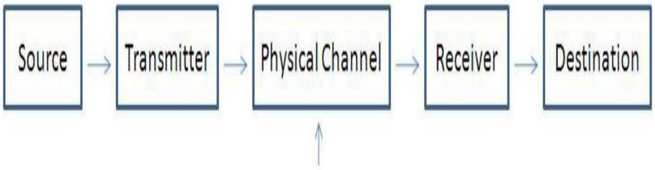

Figure 1.1 : General Communication System

- The receiver ordinarily performs the inverse operation done by the transmitter. It reconstructs the original message from the received signal.
- The destination is the system or person for whom the message is intended.

Error Detection And Correction Methods: Being introduced to the concepts of coding it is easier to explain different error detection and correction schemes. Error correction may be avoided at certain cases where retransmission is feasible and effective. But error detection is a must in all cases. Hence first some important error detection schemes are discussed. Then classification of forward error correction is described followed by some important properties of Forward Error Correction codes

Error Detection Schemes

- *Repetition scheme* -In repetition scheme the actual data is sent more than once. Inreceiver these repeated data are compared. Difference in these repeated data indicates error. Though this is the simplest way of detecting error it is not popular as it reduces the rate of actual message transmission.
- *Parity scheme* -In parity scheme all the data sets are assigned a particular parity i.e.either even or odd. In the receiver parity of received data is checked. If it does not satisfythe assigned parity, it is found to be in error. It is effective only for odd number of errors.It cannot detect even number of errors as even number of errors will leave the parityunchanged.
- *Checksum Scheme* -In this scheme a checksum is calculated in the transmitter and sent with the actual data. In receiver checksum is calculated and compared with the received checksum. A mismatch is an indication of error. If data and checksum both are received with error then the detection may not be possible.
- *Cyclic Redundancy Check scheme* - In this scheme the message is interpreted aspolynomial and is divided by a generator polynomial. Then the reminder of the divisionis added to the actual message polynomial to form a code polynomial. This codepolynomial is always divisible by the generator polynomial. This property is checked bythe receiver. If failed to satisfy this property the received codeword is in error. It iscomplex but efficient error detection scheme.
- *Hamming distance Based Check scheme* This scheme is basically parity based schemebut here parity of different combination of bits are checked for parity. It can detect doubleerrors and can correct single errors.
- *Polarity scheme* - In this scheme the actual message along with its inversion format. Inreceiver it is checked whether two sets are inverse of each other. If not it is an indication of error. It is not that popular as the code occupies double the bandwidth for the actual message. Moreover if corresponding bits in the data and is inverse are in error then it will not be able to detect the error.

III. ERROR TOLERANT TECHNIQUES FOR PARALLEL FFTS

A. Error Correction based on Hamming Codes :

The aim of error tolerant design is to protect parallel FFTs from errors. Various schemes have been proposed for error detection and correction in FFTs. One of the basic and simple methods is error correction using hamming codes. Unlike parity code which can detect only odd bit error, the hamming code can detect two bit errors and correct one error. Similar to other error correction codes, hamming codes also utilizes the parity bit which is generated for the corresponding input sequence for detecting errors . It achieves higher code rate with minimum distance of three. The number of parity bits depends on the total number of data bits. For example, hamming code with 4 information bits produces 7 encoded data bits with its difference being the parity. In this case, the three parity bits h1, h2, h3 are computed as a data bits c1, c2, c3, c4 as described below

$$h1=C1+C2+C3\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(1)$$

$$h2=C1+C2+C4\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(2)$$

$$h3=C1+C3+C4\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(3)$$

The limitations of is that, during the multiple error scenario hamming code will not be able to exactly identify the individual FFTs with error

B. Fault tolerant FFT based on Parseval's Check:

Parseval's method is one of the techniques to detect errors parallel in multiple FFT. This is achieved with Sum of Squares (SOSs) check based on Parseval's theorem. The error free FFT should have its Sum of Squares of the input equaling the Sum of Squares of its frequency domain output. This correlation can be used to identify errors with minimum overhead. For parallel FFTs, the Parseval's check can be combined with the error correction codes to minimize the area overhead. Multiple error detection and correction is achieved through this combination. One of the easy ways is to generate the redundant input for single FFT with all the four FFT inputs. To correct error the parity FFT output is XORed with fault free outputs of the FFTs. Compared to the previous schemes presented in the Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks, this technique reduced the total number of Sum of Squares used. Another existing work done is by combining SOS checks with hamming codes instead of using Parseval’s check individually as shown in Fig. 1.2

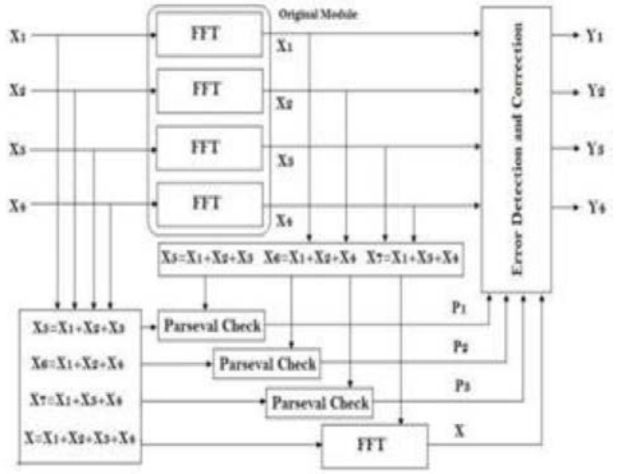

Fig.1.2 Fault tolerant FFT based on Parseval’s Check

IV. PARALLEL IMPLEMENTATION OF FFT

The computational problem for DFT is to compute the sequence {X (k)} of N complexvalues for a given sequence of data {x (n)} of length N as given in equation (3-1).

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn} \quad ,0 \le k \le N \qquad (3\text{-}1)$$

$$X(K) = \sum_{n=0}^{\frac{N}{2}-1} x_e(n) W_{N/2}^{nk} + W_N^K \sum_{N=0}^{\frac{N}{2}-1} x_o(n) W_{N/2}^{nk} \qquad (3\text{-}2)$$

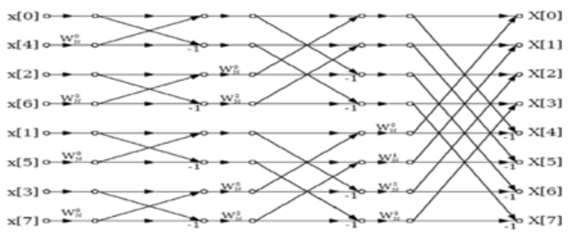

Figure 1.3: flow graph of decimation in-time fft algorithm

DFT is calculated more efficiently using the Radix-2 fast Fourier transform or FFT algorithm . Under this

The 1st term in equation (3-2) is the N/2 point DFT of the even indexed sequence and the 2nd term is the N/2 point DFT of the odd indexed sequence ($x_o(n)$). This computation is presented in Figure 1.3 The structure is typically called a butterfly structure

This architecture can be extended for larger size FFT computation of the form 2^k where k is an integer. When the FFT size is large the number of parallel computation required constantly increases. The major advantage of using GPU for FFT calculation is to perform the multiplications in parallel using the large array of low complexity processors instead of computing them sequentially. This reduces the computational time and can be used very efficiently for large sequence FFT calculation. Similar analogy can be drawn for IFFT computation in GPU. Since FFT is a major processing in LTE 3GPP and it can be implemented using parallel architecture, GPU hardware as a tool has been used for efficient implementation of this.

V. COGNITIVE ERROR CORRECTION CODES AND PARSEVAL CHECKS AND ITS APPLICATIONS

As was said in the previous section, the transmitter can have several roles together. To compress data, to secure data, to make it more reliable and lastly to transmit it as signals suited for the physical channel. Compressing data is also called source coding; it consists of mapping sequences of symbols in the original data stream to shorter ones. This is done based on the statistical distribution of the original data: the most frequent sequences are mapped to shorter ones while rare sequences are mapped to longer ones. By doing this, the resulting sequences are on average shorter, i.e. sequences with fewer symbols. On the opposite, in order to make the sequence of symbols robust to errors, redundancy is added to it. This is called channel encoding and consists of mapping shorter sequences to longer ones so that if a few symbols are corrupted the original data can nevertheless be found back. More often we need both of these. This seems contradictory since one reduces the number of sent symbols while the other increases it. However, it is not really. The source coding reduces the redundancy of unstructured data which would not provide protection if symbols were corrupted. For example, despite knowing that a message contains on average 99% of zeros, you cannot know which bits were corrupted when sending the message as it is. On the opposite, channel coding adds structured data to improve protection against such errors during the transmission. By taking the compressed message and repeating three times each bit, you can decode correctly up to one error per three bits introduced. One could wonder if a technique performing both in a single step could be more efficient than doing it sequentially. It turns out that performing source and channel coding sequentially tends to be optimal when the treated sequence length tends to infinity. This is known as the source-channel coding separation theorem and is one of the results of Shannon's ground breaking work.

For finite sequence length, such joint encoding techniques are still a subject of research. Until now, we spoke only about symbols and about mapping sequences of symbols to other sequences of symbols with better properties. However, the physical channel does not, technically speaking, transmit symbols but signals (waves, voltage, etc...). We however assume a one-toone mapping between symbols and signals which is done by a modulator to map a symbol to the corresponding signal and a demodulator mapping back a received signal to a received symbol, or information about the likelihood of each potential symbol. Notice that by separating the source and channel coding, an encryption module can also be conveniently inserted between both. All three modules: compression, encryption, channel coding are of course optional and not necessarily included in a communication system.

The part of interest for us is channel encoding and decoding. As a side note, but important, one consequence of source coding or encryption is that any of them tends to produce equal probability sequences of symbols. This argument will support an important assumption for the input of the channel encoder later on. Moreover, even if these modules are not present and nothing is known about the source's output, this is still the best assumption that can be made. The main part of interest for us is the channel encoder and decoder and it can now be isolated from the remaining system. Lastly, the modulator and demodulator constitute the glue between the transmitter, the physical channel and the receiver. The channel can be considered as the modulator, the physical channel and the demodulator together, providing an abstract model having as input and output symbols.

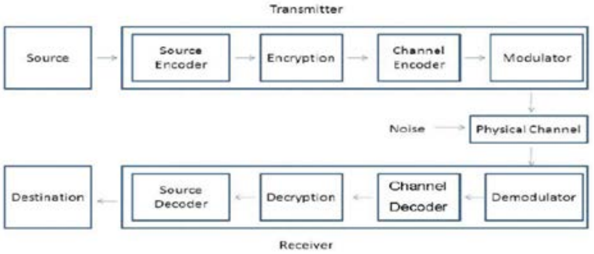

Fig 1.3 application of Communication Systems

However, the received signals, altered by noise, may not match any of the sent ones. So either it is mapped to other symbols in a bigger alphabet or some threshold decision must be used to decide which symbol of the original alphabet it should be. This is seen in more details in the section about channels

VI. LITERATURE REVIEW

SR.NO.	TITLE	AUTHORS	YEAR	METHODOLOGY
1	, "Evaluating Direct Compare for Double Error Correction Codes," in *IEEE Transactions on Device and Materials Reliability*, vol. PP	S. Liu, P. Reviriego and L. Xiao,	2017	Direct compare of information coded with error correction codes
2	Probabilistic error detection and correction in switched capacitor circuits using checksum codes	M. I. Momtaz, S. Banerjee and A. Chatterjee	2017	error detection in linear digital and analog circuits using check sum codes
3	"Timing-drift channel model and marker-based error correction coding,"	H. Kaneko,	2017	channels with imperfect synchronization. Most of the conventional coding schemes
4	Distributed decoding of convolutional network error correction codes	H. Yang and W. Guo	2017	network coding, decoding
5	Correlated insertion/deletion error correction coding for bit-patterned media	Y. Suzuki and H. Kaneko	2017	channel model and error correction coding
6	Error Correction Coding Meets Cyber-Physical Systems: Message-Passing Analysis of Self-Healing Interdependent Networks	A. Behfarnia and A. Eslami,	2017	Coupling cyber and physical systems
7	Multiple channel error-correction algorithms for LCC decoding of Reed-Solomon codes and its high-speed architecture design	L. Wang, W. Zhang, Y. Wang, Y. Hu and Y. Liu	2017	The decoding algorithms of RS code
8	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	Z. Gao	2016	algorithmic-based fault tolerance
9	Fault Tolerant Parallel Filters Based on Error Correction Codes	Z. Gao	2015	coding techniques to protect parallel filters
10	Efficient Coding Schemes for Fault-Tolerant Parallel Filters	Z. Gao	2015	Digital filters

S. Liu, P. Reviriego and L. Xiao, [1] Direct compare of information coded with error correction codes (ECCs) has been proposed to efficiently protect data comparisons against soft errors. So far it has been evaluated only for single error correction-double error detection (SEC-DED) codes. As technology scales multiple bit errors are more frequent and thus more advanced protection is needed. This letter evaluates direct compare when using double error correction (DEC) codes. The results show that it can significantly reduce the circuit overheads and that the savings are larger than when used for single error correction.

M. I. Momtaz, S. Banerjee and A. Chatterjee [2] In the past, techniques for error detection in linear digital and analog circuits using check sum codes have been developed and shown to be highly efficient. While error detection is a solved problem, error correction has proved to be difficult due to the time and area overheads involved in diagnosing failed system states and correcting them in real-time. To solve the correction problem, real-time probabilistic correction mechanisms have been proposed for digital circuits that correct for state errors in a probabilistic manner, circumventing the process of accurate error diagnosis. Such a technique is difficult to apply to continuous-time analog circuits without altering the analog transfer function, due to the nature of error feedback mechanisms involved. However, switched-capacitor circuits offer intrinsic advantages; they replicate analog continuous-time behavior while retaining the benefits of a digital clock. In this work, we show how errors in switched-capacitor circuits can be detected and corrected, using probabilistic correction algorithms, by taking advantage of the separation in time afforded by the use of a digital clock between error-free and error-affected clock cycles of the circuit. By probabilistically correcting errors in real-time before the onset of future clock cycles, the advantages offered by digital clocks are exploited to deliver high-fidelity analog performance in switched-capacitor filters resulting in significant SNR benefits at low cost.

H. Kaneko,[3] Several types of insertion / deletion / substitution error correction codings have been proposed for channels with imperfect synchronization. Most of the conventional coding schemes assume insertion/deletion errors of bit granularity, while in some applications, e.g. bit patterned media recording, insertion/deletion errors occur as a result of accumulation of small synchronization errors. This paper considers a timing-drift channel model in which a fraction of bit (i.e., 1 /ν-bit) is inserted and deleted, and describes application of conventional marker-based IDS error correction coding to the channel. Also simulation results show bit error rates of the marker-based coding.

H. Yang and W. Guo, [4] The decoding problem is addressed in this paper for the scenario that convolutional codes are employed at the source node of the network with linear or convolutional network coding for error correction. Since network errors may disperse or neutralize due to network coding, decoding cannot be done at sink nodes merely based on the minimum Hamming distance between the received and sent sequence. Source decoding is proposed in previous work by multiplying the inverse of the network transfer matrix, where the inverse is hard to compute and sometimes the result is noncausal. Starting from the Maximum A Posteriori (MAP) decoding criterion, we find that it is equivalent to the minimum error weight under our model. Inspired by classical Viterbi algorithm, we propose a Viterbi-like decoding algorithm based on the minimum error weight of combined error vectors, which can be carried out directly at sink nodes and can correct any network errors within the capability of convolutional network error correction codes (CNECC). We then study the distributed decoding of CNECC and give a sufficient condition that is able to realize such a decoding process with the proposed algorithm.

Y. Suzuki and H. Kaneko, [5] This paper presents channel model and error correction coding for correlated insertion/deletion errors in high-density magnetic recording media. Simulation results show that the bit error rate can be lowered by the presented coding.

A. Behfarnia and A. Eslami,[6] Coupling cyber and physical systems gives rise to numerous engineering challenges and opportunities. An important challenge is the contagion of failure from one system to another, which can lead to large-scale cascading failures. However, the self-healing ability emerges as a valuable opportunity where the overlaying cyber network can cure failures in the underlying physical network. To capture both self-healing and contagion, this paper considers a graphical model representation of an interdependent cyber-physical system, in which nodes represent various cyber or physical functionalities, and edges capture the interactions between the nodes. A message-passing algorithm is proposed for this representation to study the dynamics of failure propagation and healing. By conducting a density evolution analysis for this algorithm, network reaction to initial disruptions is investigated. It is proved that as the number of message-passing iterations increases, the network reaches a steady-state condition that would be either a complete healing or a complete collapse. Then, a sufficient condition is derived to select the network parameters to guarantee the complete healing of the system. The result of the density evolution analysis is further employed to jointly optimize the design of cyber and physical networks for maximum resiliency. This analytical framework is then extended to the cases where the propagation of failures in the physical network is faster than the healing responses of the cyber network. Such scenarios are of interest in many real-life applications such as smart grid. Finally, extensive numerical results are presented to verify the analysis and investigate the impact of the network parameters on the resiliency of the network.

L. Wang, W. Zhang, Y. Wang, Y. Hu and Y. Liu, [7] Reed-Solomon (RS) code is one of the most widely used error control codes. The decoding algorithms of RS code can be briefly divided into hard-decision decoding (HDD) and algebraic soft-decision decoding (ASD). However, traditional RS decoding algorithms perform unsatisfactorily over bursty channel. Therefore, many modified RS decoding algorithms utilised in bursty channel decoding were proposed. However all of them are HDD and the computation is costly. In this study, the authors propose an ASD algorithm which can be utilised both in additive white Gaussian noise channel and bursty channel. In order to be utilised in multiple channel, the proposed algorithm combines original HDD-based low-complexity chase (HDD-LCC) and burst-error correcting (BC) together. What's more, BC is also modified by adding in the mechanism of pre-judgement to reduce the iterations of BC. The modified algorithm can give a coding gain reaching up to 0.1268 and 1.33 dB compared with BC and HDD-LCC, respectively when symbol error rate (SER) is 10^{-4} in bursty channel. The proposed RS decoder is implemented and synthesised with Semiconductor Manufacturing International Corporation 0.13-μm CMOS technology library. The results show the proposed decoder can operate at 200 MHz to achieve the throughput of 1.673 Gbps.

Z. Gao *et al.*, [8] Soft errors pose a reliability threat to modern electronic circuits. This makes protection against soft errors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic-based fault tolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT. One example is fast Fourier transforms (FFTs) that are a key building block in many systems. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, probably the use of the Parseval or sum of squares check is the most widely known. In modern communication systems, it is increasingly common to find several blocks operating in parallel. Recently, a technique that exploits this fact to implement fault tolerance on parallel filters has been proposed. In this brief, this technique is first applied to protect FFTs. Then, two improved protection schemes that combine the use of error correction codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection.

Z. Gao, P. Reviriego, Z. Xu, X. Su, J. Wang and J. A. Maestro, [9] As the complexity of communications and signal processing systems increases, so does the number of blocks or elements that they have. In many cases, some of those elements operate in parallel, performing the same processing on different signals. A typical example of those elements are digital filters. The increase in complexity also poses reliability challenges and creates the need for fault-tolerant implementations. A scheme based on error correction coding has been recently proposed to protect parallel filters. In that scheme, each filter is treated as a bit, and redundant filters that act as parity check bits are introduced to detect and correct errors. In this brief, the idea of applying coding techniques to protect parallel filters is addressed in a more general way. In particular, it is shown that the fact that filter inputs and outputs are not bits but numbers enables a more efficient protection. This reduces the protection overhead and makes the number of redundant filters independent of the number of parallel filters. The proposed scheme is first described and then illustrated with two case studies. Finally, both the effectiveness in protecting against errors and the cost are evaluated for a field-programmable gate array implementation.

Z. Gao *et al.*,[10] Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters' structure and properties to achieve fault tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost.

VII. CONCLUSION AND FUTURE WORK

In this work we concludes that the vision and challenge for the convergence of the Fault Tolerant Parallel FFTs Using Error Correction Codes. The goal of the conceptual design is utilize the key features of the cognitive Error Correction as possible as it can, like the efficient spectrum utilization, software defined radio, etc. This creates new challenges for the Error Correction which have been addressed applying varies approaches as has been discussed in the previous sections. The fundamental problems in detecting the spectrum holes are naturally mostly related to signal processing at the physical layer. On the basis of this result, our future research work would include Implementation of OFDM based communication system on GPU based CUDA platform Implementation of high complexity communication system like SC-CDMA MC-CDMA, WCDMA, V-Blast etc. on GPU and performance comparison with standard architecture Development of computationally efficient algorithms for OFDM based communication systems by providing parallel implementation of FFT and IFFT. Performance analysis of multicarrier OFDM systems for WLAN, WiMAX, MCCDMA, MIMO-OFDM, LTE, 3GPP on GPU based computing platform. Implementation of signal processing algorithms for equalization, preequalization, PAPR reduction, optimization of PAPR reduction techniques and pilot carrier insertion for OFDM based system under GPU environment. Performance analysis of signal processing algorithms for wireless communication under constrained computing resources.

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