Reduction For Delay And Area Efficient Realization of FIR Filters Using RBMPPG For SDR Application

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Abstract- During this report approach of FIR Filter victimisation System Level Tools like Simulink in Xilinx System Generator and hardware primarily based FIR Filter method victimisation Verilog has been planned. Within the analysis field, the amplify demand of portable devices formulate Low power device technique. Among the integrated circuits, Power dissipation is one in all the first design objectives, once speed. The planned FIR filters design approach technique used for achieving lower adaptation delay and efficient area and delay efficient realization. The changed method delayed LMS adaptive filter consists of Weight update block with Redundant Binary Modified Partial Product Generator (RBMPPG) to attain a lower adaptation delay and efficient area. Finite impulse response (FIR) filters are utilized as channel filters in SDR (Software outlined Radio) receivers.

Keywords: Finite impulse response (FIR) filter, Least mean square (LMS) filter, Redundant Binary Partial Modified Product Generator (RBMPPG), Digital up converter (DUC), FIR interpolation filter, Root-Raised-Cosine (RRC) Architecture, VLSI (Very Large Scale Integration), Simulink and Xilinx System Generator.

I. INTRODUCTION

The 3 most generally accepted metrics for measure the performance of a circuit unit are power, delay and area. Minimizing area and delay has continuously been thought of necessary, however reducing power consumption has been gaining prominence recently. With the increasing level of device integration and therefore the growth in quality of micro-electronic circuits, reduction of power potency has come back to fore as a primary approach goal whereas power potency has continuously been fascinating in electronic circuits. Recent advances in mobile computing and multimedia applications demand high performance and low-power VLSI Digital Signal processing (DSP) systems. One amongst the foremost a wide used operation in DSP is Finite-Impulse Response (FIR) filtering. Software radios will considerably scale back the price and quality of today's cellular radio base stations. Software radios architectures centre on the utilization of wide band (WB) A/D converters and D/A converters as near the antenna as possible, with as much radio functionality as possible enforced within the digital domain. The reconfigurable FIR filters are widely employed in multiband mobile communication system. The filters exploitation in mobile communication system should be operative in low frequency and notice to consume less power and high speed. The advance technologies in mobile communication systems unit are exacting the low power and low quality techniques.

The SDR [15] technology used to replace the analog signal processing with digital signal processing so as to produce versatile reconfiguration. Approach of SDR systems is incredibly difficult as a result of it's very troublesome to design a system that preserves most of the properties of the perfect/ideal Software radio whereas being realizable with current-day technology.

II. LITERATURE SURVEY

The review was supported a range of revealed literature primarily. The timeframe is 2006 -2016. The search is expounded to applicable revealed papers on Finite impulse response filter and it's been ascertained that there's scope of any work. The computer approach may be a simple approach and hence comparatively straightforward. However the most downside is that, the amount of branches of filtering-DDC-SRC is directly proportional to the amount of received channels i.e. the quality of the computer approach is directly proportional to the amount of channels. The filters employed in the PC high area quality and so enhanced static power.

Pucker, L. in paper [2] entitled ―Channelization techniques for software defined radio planned DFT Filter Banks. DFT filter bank may be a uniformly modulated filter bank, that has been developed as associate an efficient substitute for computer approach once the amount of channels ought to be extracted is a lot of, and therefore the channels are of uniform bandwidth (for example several single standard communication channels ought to be extracted). The most advantage of DFT filter bank is that, it will with efficiency utilize the polyphone decomposition of filters. the restrictions of DFTFBs are that the channel filters have fixed equal bandwidths admire the specification of a given standard's. Several designs are planned to design low power consumption and low area and low complexity design reconfigurable FIR filter for SDR system.

Table I: Area, Delay & Power Dissipation Of Different Adder And Multiplier Topologies

<table>
<tr><th>S.No.</th><th>Description</th><th>Methodology</th><th>Result Power/Delay/Area</th></tr>
<tr><td>1.</td><td>Decimate the high frequency signal (128 KHz) upto respective low frequency signal (3.4 KHz)</td><td>MAC (Multiplier Accumulator) based FIR filter has been used</td><td>610-Multiplication per Second (MPS) & 230-(TSR) Total Storage Requirement</td></tr>
<tr><td>2.</td><td>Efficient FIR implementation</td><td>Using Kaiser and Tukey window technique</td><td>Tukey window for alpha values 0, 0.25, 0.5, 0.75 & Kaiser window for same alpha values multiply by 5</td></tr>
<tr><td>3.</td><td>FIR implementation for Low power and area efficient of Adder</td><td>ADDERS
1. Block Carry Look ahead adder (BCLA)
2. Carry Select Adder (CSA)
3. Carry Skip Adder with fixed block size (CSFBA)
4. Carry Skip Adder with Variable block size (CSVBA)
5. Conditional Sum Adder (CoSA)
6. Ripple Block Carry Look Ahead Adder (RBCLA)
7. Ripple Carry Adder (RCA)
8. Carry Increment Adder (CIA)</td><td><table><tr><th>Power Dissipation</th><th>Area</th><th>Delay ns</th></tr><tr><td>85.83mW</td><td>33.29%</td><td>20.205</td></tr><tr><td>83.88mW</td><td>39.73%</td><td>17.691</td></tr><tr><td>85.83mW</td><td>33.29%</td><td>20.083</td></tr><tr><td>83.85mW</td><td>36.51%</td><td>20.337</td></tr><tr><td>88.72mW</td><td>55.84%</td><td>13.669</td></tr><tr><td>85.83mW</td><td>33.92%</td><td>20.200</td></tr><tr><td>84.2mW</td><td>33.29%</td><td>20.205</td></tr><tr><td>92.35Mw</td><td>42.29%</td><td>27.892</td></tr></table></td></tr>
<tr><td>4.</td><td>FIR implementation for Area, delay and power dissipation of Multiplier</td><td>MULTIPLIERS
1. Booth Multiplier (BM)
2. Modified Booth Multiplier (MBM)
3. Wallace Tree Multiplier (WTM)
4. Modified Booth Encoded Wallace Tree Multiplier (MBWTM)</td><td><table><tr><th>Power Dissipation</th><th>Area</th><th>Delay ns</th></tr><tr><td>83.58mW</td><td>45.32%</td><td>42.21</td></tr><tr><td>85.39mW</td><td>51.43%</td><td>44.965</td></tr><tr><td>89.91mW</td><td>73.23%</td><td>37.859</td></tr><tr><td>85.55mW</td><td>54.87%</td><td>39.392</td></tr></table></td></tr>
<tr><td>5.</td><td>FIR filter with memory management system for frequency band selection using VHDL</td><td>1. Multirate Polyphase Decimator direct form
2. Multirate Polyphase Decimator direct form</td><td><table><tr><th>Power mW</th><th>Speed MHz</th><th>Delay ns</th></tr><tr><td>13</td><td>236.79</td><td>10.204</td></tr><tr><td>13</td><td>274.57</td><td>6.297</td></tr></table></td></tr>
<tr><td>6.</td><td>Reconfigurable pulse shaping FIR filter are low complexity and power consumption.</td><td>Multiple Constant Multiplication (MCM) using architecture of RRC FIR filter (Shift & Add unit). Interpolation factors of 4, 6, and 8 for 25, 37, and 49-taps filters respectively</td><td>28% more gate consumption</td></tr>
<tr><td>7.</td><td>Reconfigurable pulse shaping FIR filter are low complexity and power consumption.</td><td>Architecture of RRC FIR filter (Partial Product Generator unit, PPG). Implementation of five different filter lengths of 19, 25, 37, 49 and 97 with five different interpolation factors 3, 4, 6, 8 and 16</td><td>Data generator generates 7-input samples according to the interpolation factor. Technique resulted in less area and less power consumption.</td></tr>
</table>

A changed canonical signed digit (CSD) [4] is planned to design to enhance power consumption however this are obtained by the reduction of operative speed and this method is unsuitable for SDR system. Low power and low area FIR filter has been achieved by using the efficient Look up Table (LUT) however but this approach isn't applicable for higher order filter as a result of it will increase the size of read-only-memory (ROM).

Cardalli et al. [8] proposes a reconfigurable design to implement an optimized QPSK modulator for DVB-S application. This work proposes a reconfigurable design to support 3 totally different interpolation factors for various input file rates of DVB transmission standards. The disadvantage of this design is that it uses 3 Block Random Access Memories (BRAMs) that resulting high.

Another work by Gallazzi et al. [9] describes a digital multi-standard reconfigurable FIR filter to support WLAN or Wi-Fi and UMTS during a single structure. This paper suffers from the disadvantage of higher propagation delay because it adopts the MAC based mostly approach for the implementation.

Pulse shaping filters are widely used to transmit or receive the signal among a specific channel bandwidth, decrease the BER and increase the data transfer rate. Among the available pulse shaping filters, root raised cosine filters (RRC) are largely used due to its high inter-symbol interference (ISI) rejection ratio and high bandwidth limitation criteria [6-7].

Numerous designs of multipliers are planned in [3-8] and references cited in this. the standard shift-add algorithmic program is that the most elementary multiplier that produces use of repetitive shifting and accumulation of number in accordance with the multiplier. It multiplies two ‘n’ bit varietys in 'n' clock cycles and so becomes terribly protracted because the number of multiple bits increase. Although the method needs basic arithmetic operations however demands multiple clock cycles to execute. To beat this, a combinable approach consisting of logic gates and adders is given and named as array multiplier. In this, the partial product area unit generated by multiplying every multiplier bit one by one with the multiplicand. The partial product terms are then shifted in line with their bit order as outlined by shift and add algorithmic program and then are additional up to convey final output. This type of multiplier is well suited when the operand size is little, however the look complexity will increase manifolds for larger size operand.

III. DESIGN ASPECTS

3.1 Interpolation filters

An interpolation filter will increase the output sample rate by an element of L through the insertion of L-1 zeros between input samples, a method referred to as zero padding.

Fig.1: Polyphase Interpolation System consisting of an expander and LPF

Polyphase decomposition reduces the amount of operations per clock cycle by ignoring the zeros that are padded in between the first input samples. Polyphase interpolation filters give both speed and area optimization, as a result of each polyphase filter runs at the input data rate for maximum throughput.

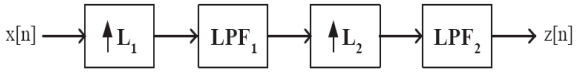

Fig.2: Interpolation System consisting of 2- expander and 2-LPF

Efficient use of Look-Up-Tables (LUTs) during this design helps to reduce the power and area whereas compared with the traditional FIR filter implementation.

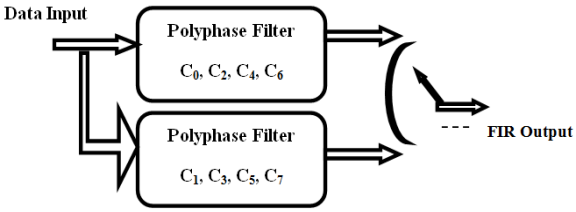

Fig.3: polyphase decomposition for interpolation filters

A. Data Generator

When the clock signal is applied to the data generator, the data has been automatically stocked with by sampling the signaling. The input data is sampled the selected value of the selection lines of multiplexer..

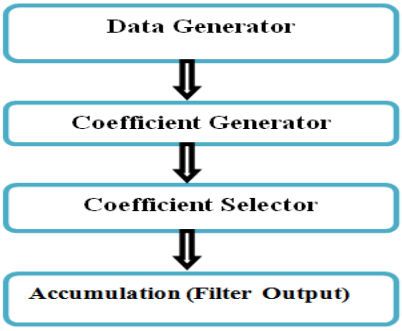

Fig.4: Representation the RRC filter.

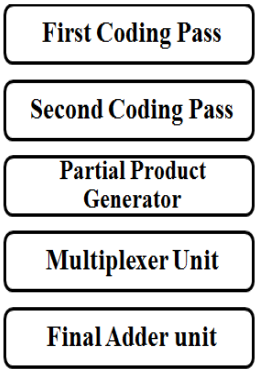

Fig.5: Coefficient Generator

B. Coefficient Generator

Coefficient generator contains of first coding pass, second coding pass, Partial Product Generator, multiplexer

unit and addition. The multiplication operation between the inputs and also the filter Coefficients is performed by coefficient generator. The hardware usage has been reduced by two-phase optimization technique. Every of the blocks in Coefficient generator are structured via multiplexer. The operation performed by the first coding pass and also the second coding pass, are similar.

(a) First Coding Pass (FCP):

For N tap filter with interpolation factor L needs (N/L) variety of convolution operations and conjointly it wants the amount of structural adders for the addition operation. If M, N, O tap filter with interpolation factor L, P, Q needs sizable amount of convolution operations and a lot of structural adders for this implementation. Henceforward for a continuing propagation delay, the area and power consumption will increase with rise in variety of multipliers and structural adders. For this, the optimization is finished by first-coding-Pass (FCP) block. During this FCP, filters variable only by the filter parameters are passed through the 2:1 multiplexer wherever the management parameter referred to as roll off factor selects the specified filter.

(b) Second coding Pass (SCP):

The selected filter coefficients from the first coding pass block are passes the second Coding pass block. Depending on the interpolation factor, filter coefficients are coded consequently.

(c) Partial Product Generator (PPG):

Shift-and-add technique is employed to get the partial product throughout the multiplication operation between the input data (X_{in}) and also the filter coefficients. In BCSE technique, realizations of the common sub expression mistreatment shift-and-add technique eliminates the common term present during a coefficient. Within the planned design, 2-bit BCSs starting from 00 to 11 are thought-about. In four of these BCSs, an adder is needed just for the pattern 11. This facilitates reduction in hardware and improvement in speed whereas perform the multiplication operation. This operation is takes place for the every and each output from the SCP i.e., this operation is performed for forty nine (49) coefficients.

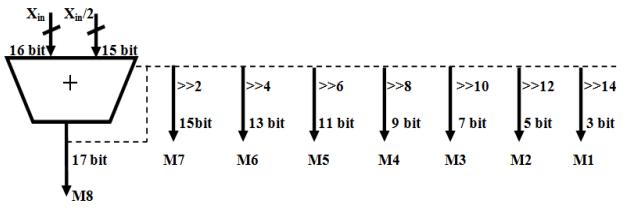

Fig.8: for PPG is shown in figure

(d) Multiplexer Unit:

The Multiplexer Unit selects the output generated from the shift and add block relying upon the coded coefficients.

(e)Addition Unit:

The addition operation may be performed by summing all the outputs of partial product generator followed by eight multiplexer units.

C. Coefficient Selector

The inputs are taken from the output of the coefficient generator that selects the specified data for process. Then the chosen inputs are then multiply the operation of AND based on the multiplexer's selection line, outputs are creates.

D. Accumulation

The inputs for accumulation were taken from the output of the data generator, Coefficient generator and Coefficient selector that are then added and also the filter output are created.

IV. PROPOSED WORK

In this paper, the power and area may be reduced using carry save adder rather than shift and add technique and conjointly the easy arithmetic adders were replaced by Redundant Binary Modified Partial Product Generator (RBMPPG). Hence, in theoretical, the architecture of the designed filter has been reduced during this design, error-correcting word (ECW) is eliminated.

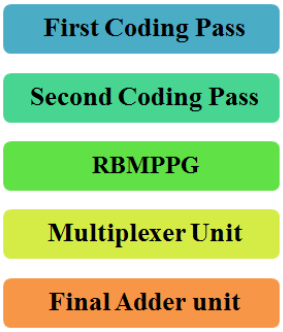

Fig.7: Coefficient Generator using RBPPG

Digital multipliers are widely utilized in arithmetic units of microprocessors, multimedia system and digital signal processors. several algorithms and architectures are planned to design high-speed and low power multipliers [1]. A Normal binary (NB) multiplication by digital circuits includes 3 steps. Within the commencement, partial product generated; within the second step, all partial product supplemental by a partial product reduction tree till 2 partial product rows stay. Within the third step, the 2 partial product rows are supplemental by a fast carry propagation adder. 2 ways are wont to perform the second step for the partial product reduction. a primary technique uses 4-2 compressors, whereas a second technique uses redundant binary (RB) numbers [10-11]. Each ways permit the partial product reduction tree to be reduced at a rate of 2:1. The redundant

binary variety illustration has been introduced by Avizienis [1] to perform signed-digit arithmetic; the RB number has the aptitude to be drawn in numerous ways in which. Fast multipliers may be designed using redundant binary addition trees [2-3]. The redundant binary illustration has conjointly been applied to a floating-point processor and enforced in VLSI [4]. High performance metal multipliers became well-liked attributable to the advantageous options, like high modularity and carry-free addition [10].

V. ANALYSIS AND SCOPE OF WORK

Researchers conclude that abundant work has not been done to cut back the quantum value, delay, araa and power thus more work will be done to cut back these parameters. Compared with CRBBE-2, the projected styles will scale back the PDP by over 14% for all cases. Compared with RBBE-4, the projected styles will scale back the PDP by up to 59.6% for the case of a 32×32-bit multiplier, and overall cases the projected design will reduce the PDP by over 30%. Thus, these results ensure the projected RBMPP-2 will be terribly helpful for coming up with area and PDP efficient RB multipliers. The performance of varied 2-bit RB multipliers using the projected RBMPPG-2 is assessed; the results area compared with NBBE-2, CRBBE-2 and RBBE-4 [14] Multipliers that area unit the newest and best styles found within the technical literature. However, more research worker interest could also be to propose new ways which will be wont to replace existing ones, leading to decrease of quantum value and different parameters.

VI. CONCLUSION

The projected design appears to be remarkably appropriate for next generation multi-standard reconfigurable DUC of SDR system projected coming up with a root-raised-cosine finite-impulse response filter for multi-standard DUC for 5 completely different standards. a replacement changed RBPP generator has been projected during this paper; this style eliminates the extra ECW that's introduced by previous styles. Therefore, a RBPP accumulation stage is saved attributable to the elimination of ECW.

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