64-Bit Carry Select Adder

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Abstract *Adders are the basic unit for performing the arithmetic and logical operation. There are main three key parameters delay, area and power consumption which should be considered while designing an adder. Carry select adder is faster than the ripple carry adder and carry look ahead adder. This adder also consumes more area to overcome that problem modified carry select adder designed. The simulation results observed using XILINX 14.3 Virtex 4.*

Keywords: CSA, VHDL, Virtex.

1. INTRODUCTION

Now a day's adders are used as vital part in many fields such as digital electronics, very large scale integration technology, Digital signal processing, and microprocessor. Adder is a combinational digital circuit which performs arithmetic and logical operation. The most basic arithmetic operation is the addition of two binary digits, i.e. bits. Speed, power, area is the key parameters in designing any adder. In the present day technical world scheming an adder is not a big pact primarily focused on the performance parameters. Before manufacturing any circuit or component designer tries to centre on the performance parameters.

1.1 Carry Select Adder

Carry select adder is based on the principle to calculate sum that is based on assuming input carry from previous stage.

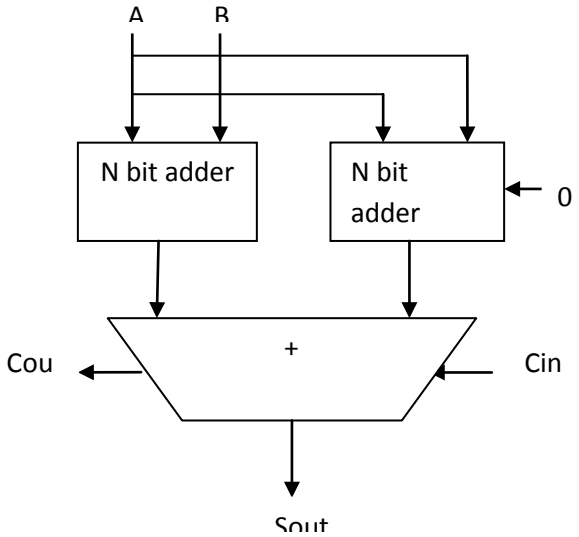


Figure 1: Carry Select Adder

One adder calculates the sum assuming input carry of 0 while the other calculates the sum assuming input carry of 1. Then, the actual carry triggers a multiplexer that selects the appropriate sum. The below given figure uses two ripple carry adder one with carry 0 and other

As discussed above there was two blocks of adders one with input 1 and second with input 0.The two blocks uses the ripple carry adder due to which circuit complexity increases as the bit length go on increasing to overcome that problem one ripple adder replaced with binary to excess converter by which circuit complexity reduces**.**

2. METHODOLOGY

Adders are the basic unit to perform arithmetic and logic operation. Different types of adders has been designed each having its own benefits and limitations.

To Design the adders based on FPGA, procedure is:

1. To study the adder with their benefits and limitations.
2. After making comparison write VHDL code.
3. Implementation and Synthesize on the Xilinx ISE Design Suit 14.3, ISim simulator.
4. After synthesization observe the simulation results.

Software to be used:

Digital Design Tools: Xilinx ISE Design Suit 14.3 , ISim simulator ,

FPGA Development board: Xilinx virtex4.

3. SIMULATION RESULTS

3.1 RTL view for 64 bit carry select adder

RTL is register transfer level, it represent the path through which data transfer take place.

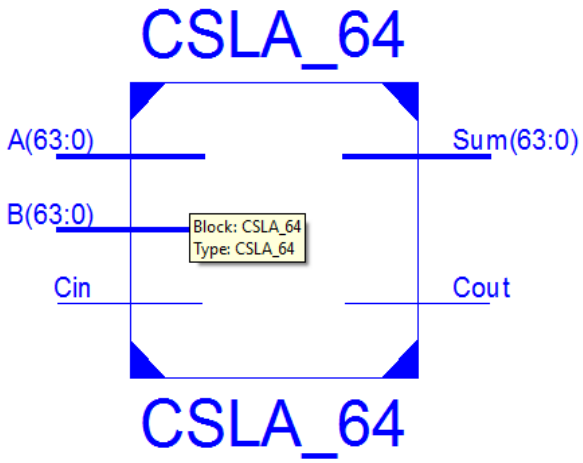


Figure 2: RTL view for 64 bit CSA

Two inputs A and B 64 bit wide and third is the carry input which can be either 0 or 1 producing the sum and cout as

output. Register-transfer-level abstraction is used in hardware description language (HDLs) like verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design.

3.2 Internal view for 64 bit carry select adder

Internal view describes how the circuit connected internally. For 64 bit carry select adder two 32 bit adders are used.

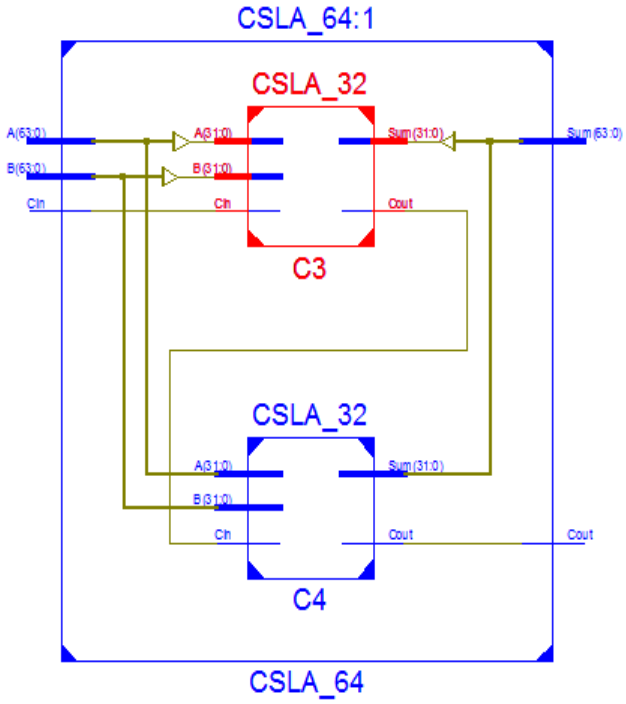


Figure 3: Internal View for 64 bit CSA

3.3 Technology view for 64 bit carry select adder

Technology view represents which technique is used. It consists of n number of blocks each one show its corresponding K-map, logic equations, truth table and circuit etc.Blocks are connected with each other.

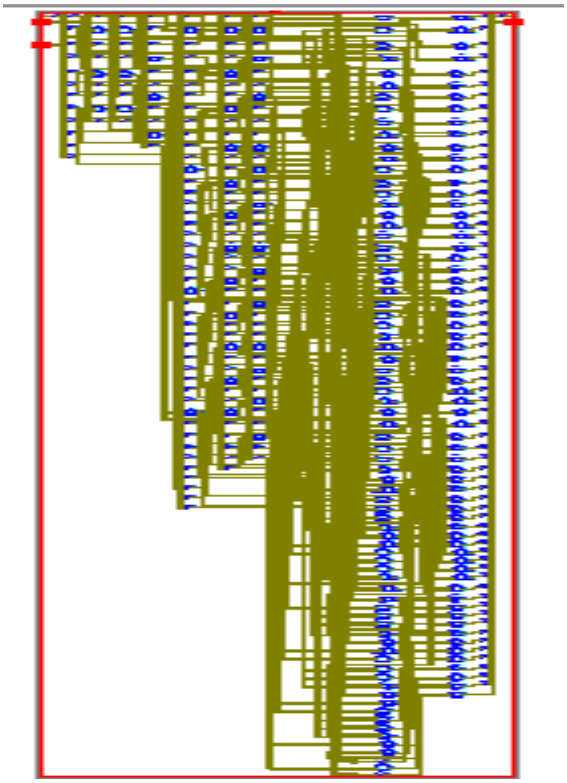
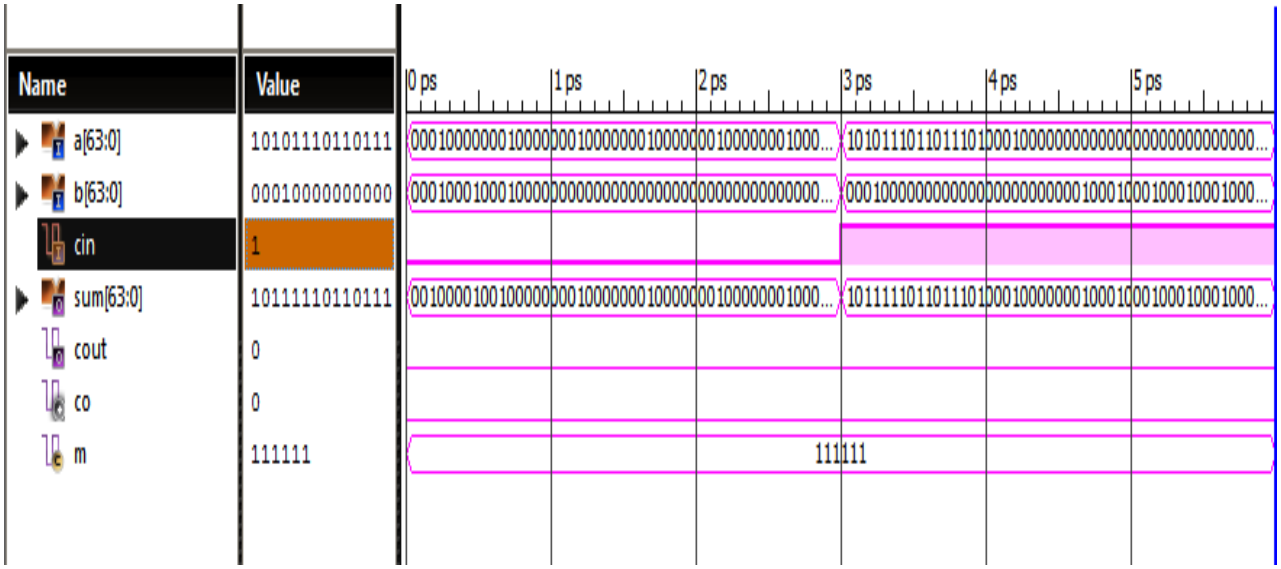


Figure 4: Technology View

3.4 Simulation result for 64 bit carry select adder

Simulation results for 64 bit carry select adder are shown below. Here two numbers which are 64 bit wide are taken after addition final result is produced.



Simulation result when carry is 0

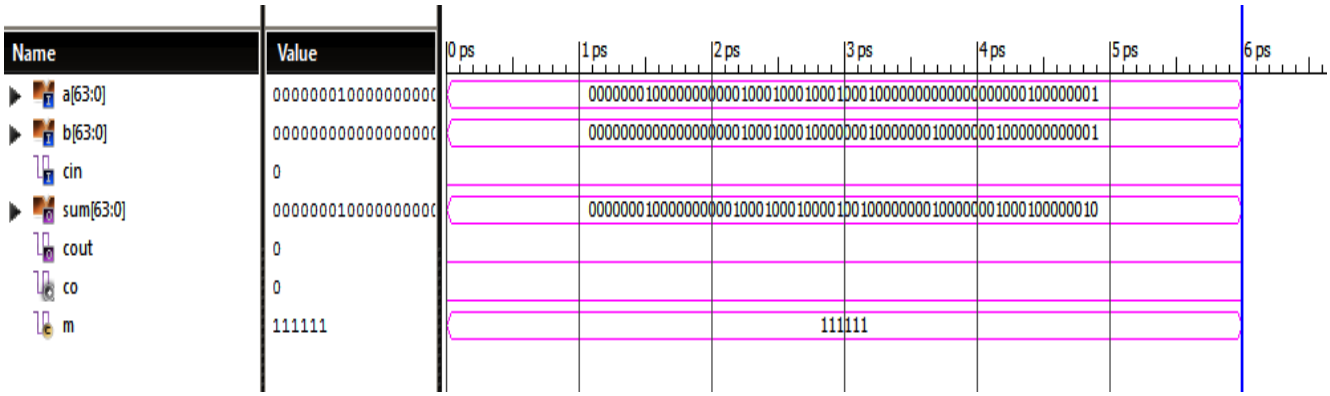


Table 1: device utilization area

Parameters	Used	Available	Utilization
No. of slices	93	6144	1%
No. of LUTs	164	12288	1%
No. of IOB	194	240	80%

The table above given presents the total utilization area or can say total chip area consumed by an adder. From the table it is clear available number of component are enough where as their utilization is negligible. Utilization of number of input output is high.

CONCLUSION

Carry select adder is faster adder but consume more area than carry look ahead adder. But with the modified carry select adder area get reduced .Delay for the 64 bit CSA is very less in comparison with the other adders.

FUTURE SCOPE

In future more parameters can be added to check its performance. It can be extended for more no of bits.

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AUTHOR'S PROFILE

Daljit Kaur has received his Bachelor of Technology degree in Electronics & Communication Engineering from SBBSIET Padhiana, Jalandhar in the year 2009. And M.Tech from DAVIET Jalandhar in year 2014 in ECE (VLSI). MY area of interest is Digital Electronics and Microprocessor.