Efficient Mismatch Calibration using Chebyshev Filter in TI-ADC

Shraddha Patel[1], Prof. Jitendra Kumar Mishra[2]

[1]*M-Tech Research Scholar,* [2]*Research Guide,, Department of Electronics & Communication*

Patel College of Science & Technology, Bhopal

Abstract – Now a days a communication system, has an essential operation of conversion of analog signals into the digital form for the processing of signal information. Therefore all the devices uses analog to digital converter (ADC) chips, these are Integrated Circuits (ICs). At the time of manufacturing process these ICs are not made identical (as it is) for conversion operations. As the result the output of multi-channel TI-ADC system get affected with the different mismatches as frequency mismatch, time mismatch, gain mismatch and offset mismatch. These mismatched needs to be calibrated for proficient functioning of the system. In the similar context in this research article an efficient mismatch calibration methodology has been proposed for utilizing the Fx-LMS algorithm and Chebyshev FIR Filter with Order 21. The figure of merit is SFDR which shows the efficiency of the calibration methodology, here we have achieved.

Keywords - SFDR, TI-ADC, Digital Filter, Mismatch Calibration.

I. INTRODUCTION

An analog-to-digital converter (ADC) samples a continuous-time analog signal at a predefined rate (sampling rate) to generate a discrete-time sequence of samples. The analog value of each sample is then represented using a finite number of bits (resolution). The sampling rate of the ADC is selected depending on the bandwidth of the analog input signal. There exist many ADC architectures that are suitable for different ranges of sampling rates and resolutions [1]. Analog-to-digital converters used in applications like communication systems and high-speed digitizers should support very high sampling rates and/or resolutions [2]. In such cases, implementing a single high-sampling rate ADC is quite challenging and at times infeasible. A popular technique to increase the effective sampling rate is to have multiple ADCs in a time-interleaved fashion with each ADC operating at a lower sampling rate [3]. In theory, by time-interleaving the outputs of M channel ADCs, a time interleaved analog-to-digital converter (TI-ADC) can achieve the same resolution as that of the individual ADCs but with M times higher sampling rate. However, in practice, the channel ADCs suffer from no idealities such as gain, offset, and timing errors. These no idealities manifest mainly due to analog circuit imperfections caused by variations in manufacturing process, voltage, and temperature [4]. Also, the reduced feature size of transistors in advanced manufacturing processes make within-die and die-to-die variations more pronounced due to the limited accuracy of the existing lithography techniques [6]. Due to the random nature of the variations [5], each channel ADC exhibits different levels of no idealities which causes channel mismatch errors in TI-ADCs. In a TI-ADC with mismatch errors, the output is a no uniformly sampled signal which degrades the achievable resolution at the output of the TI-ADC [4]. Thus, in order to retain the achievable resolution, TI-ADC implementations must either avoid mismatches between the channel ADCs through careful analog circuit design [7] or use calibration wherein the mismatch errors are estimated and then compensated for. The former approach is extremely challenging especially in newer digital-friendly chip manufacturing processes. Hence, TI-ADC implementations often rely on calibration to mitigate the effects of channel mismatch errors. The mismatch errors can be broadly classified into linear and nonlinear mismatch errors [9]. Linear mismatch errors include gain, offset, timing skew, and frequency response mismatches whereas nonlinear mismatch errors occur due to mismatches in the nonlinearity of the channel ADCs. In this thesis we consider only linear mismatch errors which typically dominate. More specifically, since gain and offset errors can be easily compensated, here we deal with only time-skew mismatch errors which occur as a result of nonuniform time skews between the sampling clocks of the channel ADCs. In practice, the time-skew errors can be assumed to be frequency independent only up to a certain output resolution and bandwidth. In high-speed TI-ADCs, the time-skew errors are frequency dependent. Thus, to achieve very high resolutions, each channel in a high-speed TI-ADC is modeled as a general frequency response and the calibration block should compensate for the frequency-response mismatch errors. All communication is getting faster and faster. Therefore, the demand for high data rate wireless digital communication is high and research into 60GHz communication and above with several GSps data rate is done. The data rate of the wireless digital communication is limited by the sampling rate and the accuracy of the data converters. Other applications are fast and accurate oscilloscopes that are designed to measure signals in the GHz range.

These applications require high bandwidth analog to digital converters (ADCs) with high accuracy and high sampling rate. These requirements are difficult to realize in a single ADC.

Therefore, Black and Hodges proposed the Time-Interleaved ADC (TI-ADC) architecture [1] in 1980. Since then lots of research has been done into the possibilities of TI-ADCs. The time-interleaving architecture brings some problems with respect to mismatch between its channels.

There are three main mismatch problems: gain-mismatch, offset-mismatch and timing-mismatch. Since TI-ADCs are mainly used in high frequency applications, where the timing-mismatch is dominant, timing-mismatch is the most challenging problem.

II. TIME-INTERLEAVED ADC MODEL

Analog-to-digital converters supporting very high sampling rates often use time-interleaving of multiple ADCs to reduce the requirements on the individual ADCs. In an M-channel TI-ADC, the continuous-time signal xa(t) is sampled using M parallel ADCs as shown in Fig. 2.1(a) [3]. The sampling clocks to the channel ADCs are applied in such a way that, at any given time instant, only one channel ADC samples the input. In an ideal TI-ADC, the mth channel ADC samples the input xa(t) as shown in Fig. 2.1(b).1 In this case, since $x_m(\nu) = x_a(\nu MT + mT) = x(\nu M + m)$, the output of the mth channel ADC $x_m(\nu)$ may be considered as being obtained from the uniform-sampling sequence $x(n)$ as shown in Fig. 2.1(c) where $z = e^{j\omega T}$. Hence, as discussed in Section 1.1.5, the Fourier transform of the downsampled sequence $x_m(\nu)$ can be written as

$$X_m\left(e^{j\omega T}\right) = \frac{1}{M}\sum_{k=0}^{M-1} e^{j\frac{\omega T-2\pi k}{M}m} X\left(e^{j\frac{\omega T-2\pi k}{M}m}\right) \quad (2.1)$$

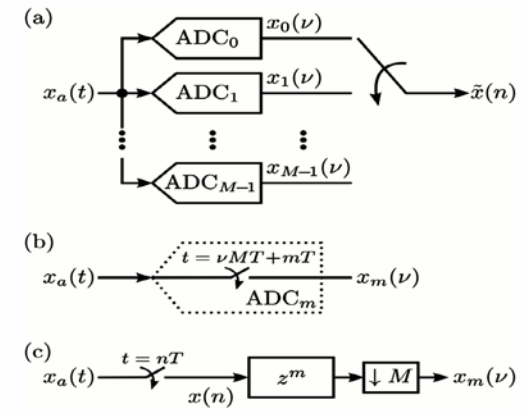

Figure 2.1: (a) Ideal M-channel TI-ADC. (b) Block diagram of the mth channel ADC. (c) Equivalent representation of (b).

TI-ADC is to make a fast ADC out of several relatively slow sub-ADCs working together in time-multiplexed mode. The basic concept of a *M* channel TI-ADC is shown in figure 2.2. In this figure *x*(*t*) is a time-continuous and amplitude-continuous signal which is fed to *M* sample and holds (S&H). Each S&H takes a sample at time *Øi* (*i* from 0 to M_i1). Ideally the sample moments are equidistant with time *Ts*.

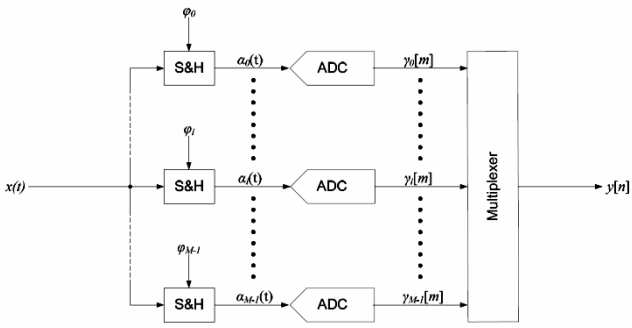

Figure 2.2: Basic Time-Interleaved ADC.

The three most common ADC problems are described in this section, they are sampling jitter, quantization noise and nonlinearity. There has already been a lot of research into these problems and several solutions are available. Therefore, these problems are taken notice of, but will not be considered in the error correction algorithm.

Quantization Noise:

Quantization noise is the error introduced by the amplitude discretization of the signal and is therefore signal dependent `noise', but can be considered to be stochastic noise under the following conditions: transitions equally distributed in time, many transitions and equal quantization steps.

The noise power under these conditions is $q2=12$, where q is the quantization step size. Since q is inversely proportional to the number of bits this error decreases when more bits are used.

Nonlinearity:

ADCs and S&Hs have certain nonlinearities. Their static nonlinearities are expressed in integral nonlinearity (INL) and differential nonlinearity (DNL). For periodic input signals nonlinearities show up in the frequency spectrum as harmonic distortion tones and determine, a.o., the spurious free dynamic range (SFDR) and the signal to noise and distortion ratio (SNDR).

Offset Mismatch:

For the discussion about offset-mismatch the offset errors are assumed to be different for each channel, and all other characteristics are the same. Offset is a DC error per sub-ADC which becomes periodic with time-interleaving.

Therefore, the offset-mismatch is periodic with period *MTs* and independent of the input signal. In the frequency-domain the offset-mismatch appears as tones at frequencies independent of the input frequency and independent of the input amplitude.

Gain Mismatch:

For the discussion about gain-mismatch the gain errors are assumed to be different for each channel, and all other characteristics are the same. The errors also occur with a period of *MTs*, just as offset mismatch, but the errors are amplitude modulated with the input frequency -0. The largest absolute errors occur at the peaks off the input signal.

Timing Mismatch:

For the discussion about timing-mismatch, the timing error, due to clock-skew, is assumed to be different for each channel, and all other characteristics are the same. The errors again occur with a period of *MTs* and are amplitude modulated with the input frequency -0 just as the gain-mismatch. The largest errors occur at the largest slew-rate of the sine wave.

III. PROPOSED METHODOLOGY

The proposed TI-ADC mismatch calibration methodology is explained below.

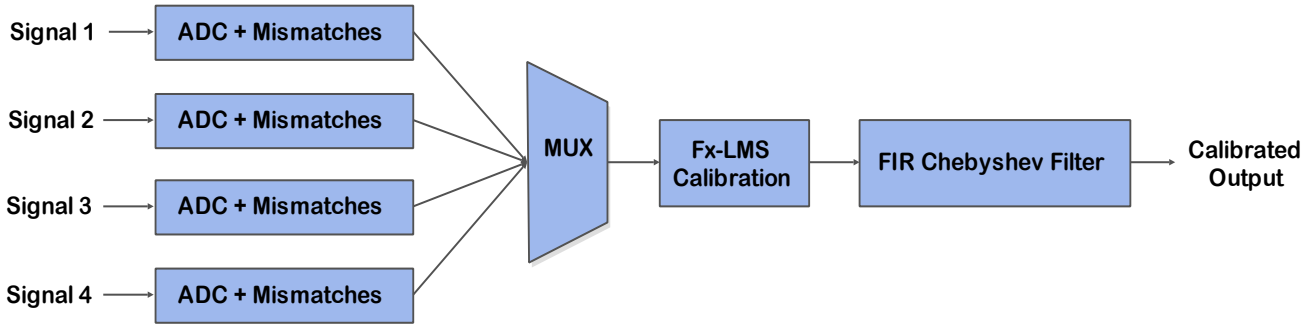

Fig. 3.1 Block Diagram of The Proposed Methodology

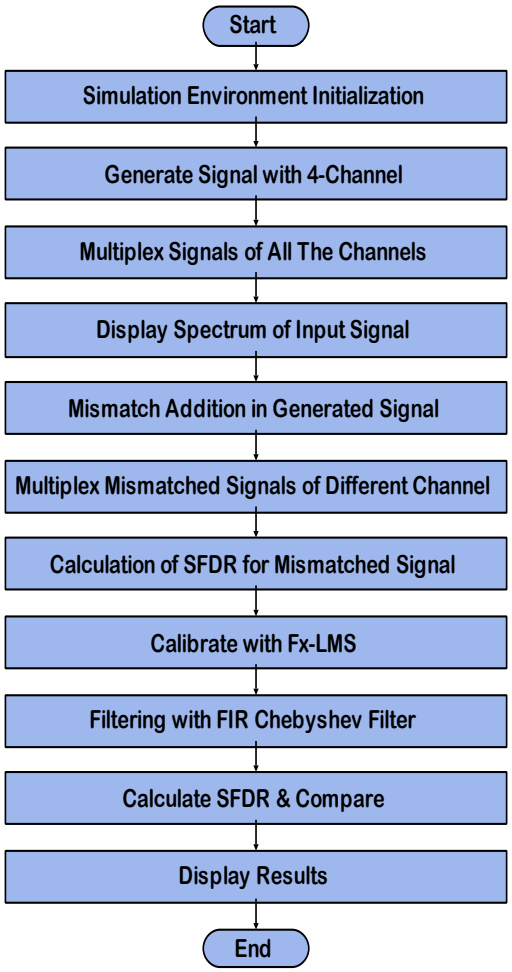

Fig. 3.2 Flow Chart of The Proposed Methodology

The block diagram of the proposed system is shown in Fig. 3.1. Here we have used 4-Channel TI-ADC system with multiplexer followed by calibration techniques first is Fx-LMS followed by Chebyshev FIR Filter.

Above system is implemented on the simulation tool and the program flow of algorithm is shown in Fig. 3.2 with the help of Flow chart.

The above flow chart is showing step by step executing of the computer algorithm.

IV. SIMULATION RESULTS

The simulation results are shown in the below figures. The comparison of the system performance is shown in table below.

Table I: SFDR Comparison

Methodology	SFDR (dB)
Proposed Methodology	78.88 dB
Previous Work	77.50 dB

From the above table it is clear that the spurious free dynamic range (SFDR) for the proposed approach is better than the previous work.

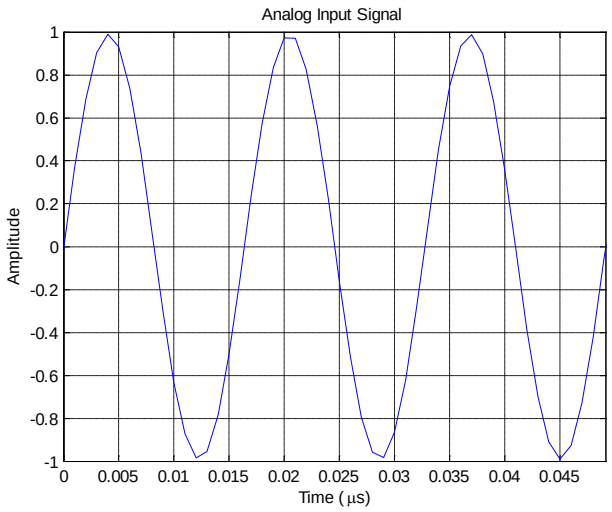

Fig. 4.1 Input Analog Signal

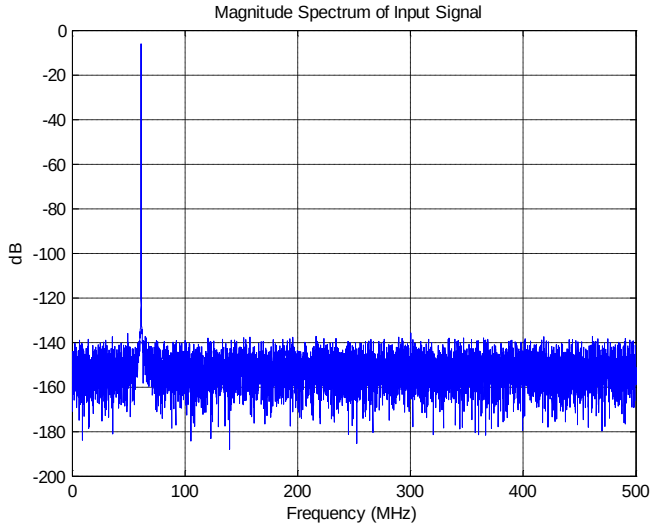

Fig. 4.2 Magnitude Spectrum of Input Signal without mismatches

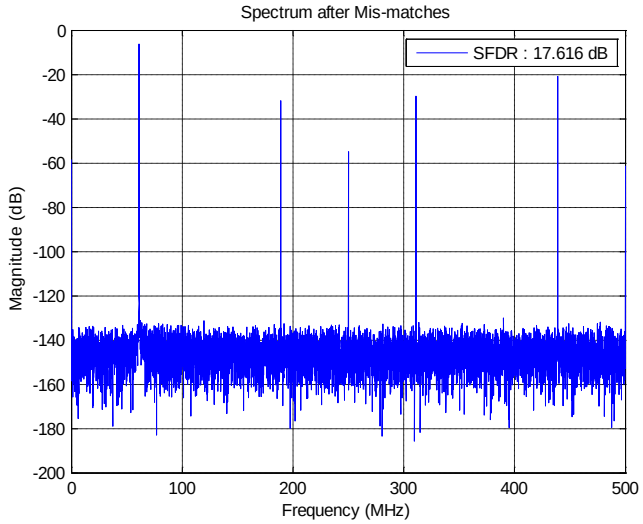

Fig. 4.3 Magnitude Spectrum of Input Signal with mismatches

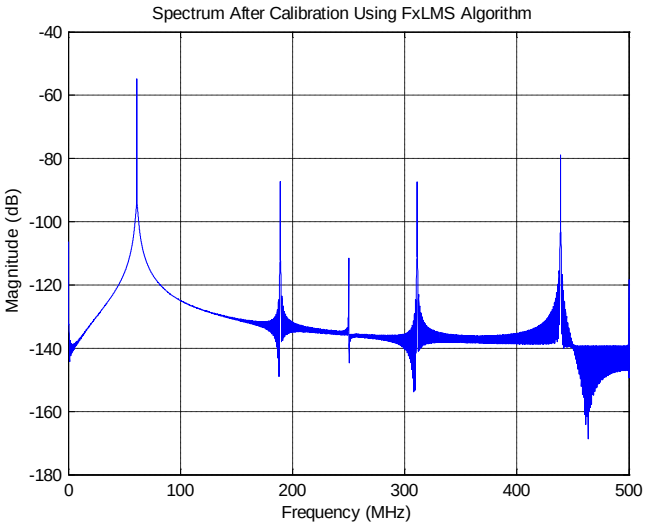

Fig. 4.4 Magnitude Spectrum of Calibrated Signal using Fx-LMS Algorithm

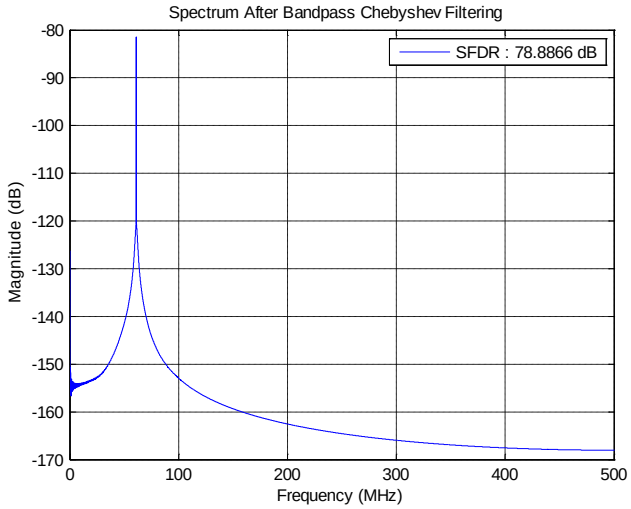

Fig. 4.5 Magnitude Spectrum of Final Output Calibrated Signal using Chebyshev Filtering

V. CONCLUSION AND FUTURE SCOPE

The time interleaved analog to digital converter system is proposed in this paper has the optimized version of the calibration structure than the previous methodologies. Our approach is simplified version and has two stages only. first one is filtered least mean square algorithm which is a kind of feedback system and further mismatched calibrated with the utilization of the Chebyshev FIR Filter. From whole discussion the proposed approach proved to be good for futuristic TI-ADC systems and as well also shown the different direction of non-complex calibration structure. Such approach also perform better with the utilization of filter banks and other series techniques which will make system little bit complex but offer better performance.

REFERENCES

[1] C.C. Boucher, S.J. Elliott, and P.A. Nelson. Effect of errors in the plant model on the performance of algorithms for adaptive feedforward control. In Proceedings of Institution of Electrical Engineers, volume 138, pages 313–319, 1991.

[2] Petraglia and S. Mitra, "Analysis of mismatch effects among A/D converters in a time-interleaved waveform digitizer," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 5, pp. 831–835, Oct. 1991.

[3] S.J. Elliott and P.A. Nelson. Multiple-point equalization in a room using adaptive digital filters. Journal of audio engineering society, 37(11):899–907, November 1989.

[4] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time interleaved ADC systems," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, pp. 261–271, Mar. 2001.

[5] F. Maloberti, "High-speed data converters for communication systems," *IEEE Circuits Syst. Mag.*, vol. 1, no. 1, pp. 26–36, 2001.

[6] S.J. Elliott and P.A. Nelson. Active noise control. IEEE signal processing magazine, pages 12–35, October 1993.

[7] D.R Morgan. An analysis of multiple correlation cancellation loops with a filter in the auxiliary path. IEEE Transactions on Acoustics, Speech and Signal Processing, ASSP-28(4):454–467, August 1980.

[8] P.A. Nelson and S.J. Elliott. Active Control of Sound. Academic Press, Inc, 1992.

[9] B. Widrow and S.D. Stearns. Adaptive Signal Processing. Prentice-Hall, 1985.

[10] L. H°akansson, I. Claesson, and P-O. Sturesson. Adaptive feedback control of machinetool vibration based on the filtered-x lms algorithm. International Journal of Low Frequency Noise, Vibration and Active Control, Accepted, 1997.

[11] J. Elbornsson, F. Gustafsson, and J.-E. Eklund, "Analysis of mismatch noise in randomly interleaved ADC system," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP'03)*, vol. 6, pp. 277–280.

[12] T.-H. Tsai, P. Hurst, and S. Lewis, "Bandwidth mismatch and its correction in time-interleaved analog-to-digital converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 10, pp. 1133 -1137, Oct. 2006.

[13] P. Satarzadeh, B. Levy, and P. Hurst, "Bandwidth mismatch correction for a four-channel time-interleaved A/D converter," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS 2007)*, pp. 1705–1708.

[14] C. Vogel, "The impact of combined channel mismatch effects in timeinterleaved ADCs," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 415–427, Feb. 2005.

[15] G. Leger, E. Peralias, A. Rueda, and J. Huertas, "Impact of random channel mismatch on the SNR and SFDR of time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 140–150, Jan. 2004.

[16] M. Seo, M. Rodwell, and U. Madhow, "Comprehensive digital correction of mismatch errors for a 400 Msamples/s 80-dB SFDR time-interleaved analog-to-digital converter," *IEEE Trans. Microw. TheoryTech.*, vol. 53, no. 3, pp. 1072–1082, Mar. 2005.

[17] S. Mendel and C. Vogel, "A compensation method for magnitude response mismatches in two-channel time-interleaved analog-to-digital converters," in *Proc. 13th IEEE Int. Conf. Electron., Circuits Syst. (ICECS'06)*, pp. 712–715.

[18] S. Mendel and C. Vogel, "On the compensation of magnitude response mismatches in m-channel time-interleaved ADCs," in *IEEE Int. Symp. Circuits Syst., 2007 (ISCAS 2007)*, pp. 3375–3378.M. El-Chammas and B. Murmann, "General analysis on the impact of phase-skew in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 902–910, May 2009.

[19] B. Murmann, C. Vogel, and H. Koeppl, "Digitally enhanced analog circuits: System aspects," in *Proc. 2008 IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008, pp. 560–563.

[20] C. Vogel and S. Mendel, "A flexible and scalable structure to compensate frequency response mismatches in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2463–2475,Nov. 2009.

[21] S. Saleem and C. Vogel, "Adaptive compensation of frequency response mismatches in high-resolution time-interleaved ADCs using a low-resolution ADC and a time-varying filter," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS 2010)*, pp. 561–564.

[22] M. Seo, M. Rodwell, and U. Madhow, "Generalized blind mismatch correction for two-channel time-interleaved A-to-D converters," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP 2007)*, vol. 3, pp. 1505–1508.

[23] M. Seo and M. Rodwell, "Generalized blind mismatch correction for a two-channel time-interleaved ADC:Analytic approach," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS 2007)*, pp. 109–112.

[24] H. Johansson, "A polynomial-based time-varying filter structure for the compensation of frequency-response mismatch errors in time-interleaved ADCs," *IEEE J. Sel. Topics Signal Process.*, vol. 3, no. 3, pp. 384–396, Jun. 2009.

[25] C. Vogel and H. Johansson, "Time-interleaved analog-to-digital converters: Status and future directions," in *Proc. 2006 IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2006, pp. 3386–3389.

[26] T.-H. Tsai,P. J.Hurst, and S. H. Lewis, "Correction of mismatches in a time-interleaved analog-to-digital converter in an adaptively equalized digital communication receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 2, pp. 307–319, Feb. 2009.