# Review: VHDL Based NOC Router Architecture

[1]Ruchika Chandravanshi, [2]Vivek Tiwari
[1,2] *Dept Electronics & communication, SIRTS, Bhopal (M.P.) India*

***Abstract - With the technological advancements a large number of devices can be integrated into a single chip. So the communication between these devices becomes vital.Because of the common bus architecture in SOC system, performance becomes sluggish which limits the processing speed. The network on chip (NoC) is a technology used for such communication. The characteristics of NOC such as scalability, flexibility, high bandwidthhave been proposed as a valid approach to meet communication requirements in SoC, where common bus architecture replaced by network.The paper addresses the design and verification of router for Mesh topology using Verilog HDL which supports five parallel connections at the same time.It uses store and forward type of flow control and FSM controller deterministic routing which improves the performance of router.Another paper focuses onthe implementation and the verification of a five port router. The building blocks of the router are buffering registers, demultiplexer, First In First Out registers, and schedulers. The scheduler uses the round robin algorithm. The proposed architecture of five port router is simulated in Xilinx ISE 10.1 software. The source code is written in VHDL.***

***Keywords - NOC, VHDL, Router Architecture.***

## INTRODUCTION

In old era ICs have been designed with dedicated point to point connections, with one wire dedicated to each signal. Due to this, large design had some limitations from physical design viewpoint. The wires (wire bus) occupy large area of chip and in CMOS technology, interconnection dominates performance and dynamic power dissipation. Network on Chip (NoC) is a new paradigm to make the interconnections inside a System on Chip (SoC) system. It reduces complexity of designing wires and also increases speed and reliability. NoC can provide separation between computation and communication supports modularity and IP reuse via standard interfaces, serve as a platform for system test, handles synchronization issue, and, hence increasing engineering productivity. In NoC technology the bus structure is replaced with a network which is a lot similar to the Internet. Segments communicate with each other by sending packetized data over this network. Network on Chip gives solution that the inter process communication among different modules takes place by transfer of packets instead of polling or arbitration as in bus architecture. The NOC design paradigm has been proposed as the future of ASIC design. There are three main components of NoC namely router, resource and resource to network interface. For the efficient NoC architecture, the router should be efficiently design as the router is the central component of the network on chip system. It is the communication backbone of the NOC system. Routers are used on a network for directing the traffic from source to the destination. It co-ordinates the data flow which is very crucial in communication network. The communication on network on chip is carried out by means of router. The goal of this paper is to provide efficient router architecture for efficient NoC Mesh Topology having five input port and five output port. The router we present in this paper supports five parallel connections at the same time. One port is the local port used to assure communication between the processing element and the router via the network interface. But for the network communication we are not consider this port in our paper. The remaining ports allow connecting the router with its neighbors. It uses store and forward type of flow control. The switching mechanism used here is packet switching which is generally used on network on chip. In packet switching the data transfers in the form of packets between co-operating routers and independent routing decision is taken. The store and forward mechanism is best because it does not reserve channels like circuit switching and thus does not lead to ideal physical channels. The Controller design in this paper is FSM Controller so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides. We design here the router which support for the communication of Mesh topology which has five input and five output ports. And for the transmission of data round robin scheduling is used.

## NETWORK ON CHIP - A BACKGROUND

The scaling of chip technologies has enabled large scale SoCs, where all components of an electronic design are integrated on a single chip. In SoCs the communication systems used are conventional bus systems and point-to-point links.

Since these two alternatives are not suitable for highly complex systems, new approaches for intrachip

communication are adopted to achieve high performance in SoCs. NoC is one such approach where communication between processors, memories, IPs, and IOs is achieved by exchanging data packets using a network. The NoC approach borrows concepts and techniques from the well-established domain of computer networking. Fig. 1 shows some basic communication structures in SoC designing. The solutions for SoC communication structures have generally been characterized by custom designed ad hoc mixes of buses and point to point links. The bus builds on well understood concepts and is easy to model. In a highly interconnected multicore system it can quickly become a communication bottle neck as more units are added to it.

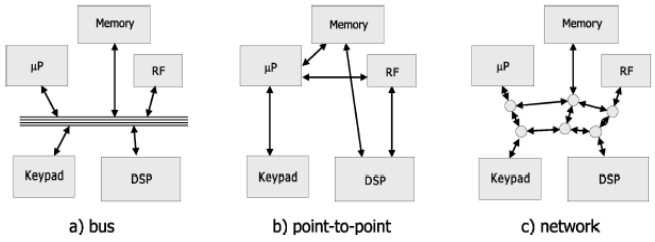


Fig. 1. Communication structures in SoC a)traditional bus based communication, b)dedicated point to point links c)network on a chip [7]

There are various advantages of networks over buses. In bus communication systems every unit attached adds parasitic capacitance, therefore electrical performance degrades as system grows. Bus timing is difficult in a deep submicron process. Bus arbitration can become a bottleneck. The arbitration delay grows with the number of masters. The bus arbiter is instance-specific. Bus testability is problematic and slow. The bandwidth for communication is limited and shared by all units attached. In network based communication only point-topoint one-way wires are used, for all network sizes, thus local performance is not degraded when scaling. Network wires can be pipelined because links are point-to-point. Routing decisions are distributed, if the network protocol is made noncentral. The same router may be reinstantiated, for all network sizes. Locally placed dedicated built in self test mechanism is fast and offers good test coverage. The aggregated bandwidth scales with the network size[3]. The NoC paradigm is highly suited to provide SoC platforms scalable and adaptable over several technology generations. NoC platforms may allow the design productivity to grow as fast as technology capabilities and may eventually close the design productivity gap[4].

## AN OVERVIEW OF NOC DESIGN APPROACH

Switching method, Topology and Routing algorithm are three important things in the design of NoC.

A. Switching Technique: Circuit switching and packet switching are two major switching techniques. Packet switching is better than circuit switching as it does not reserve the path like circuit switching.

Packet switching is utilized in most of NoC platforms because of its potential for providing simultaneous data communication between many source-destination pairs. Further it can be classified into Store and forward, Virtual cut through and Wormhole switching [5].

B. Topology: Topology defines how nodes are placed and connected, affecting bandwidth and latency of a network. Many different topologies have been proposed [6][7]. Such as mesh, torus, octagon, SPIN etc. Some researchers have proposed application specific topology that can offer superior performance while minimizing area and energy consumption. Most common topology is 2-D Mesh due to its grid-type

shapes and regular structure which are the most appropriate for the two dimensional layout on a chip. Mesh topology is easy to implement as all nodes are equally distance as shown in Figure.2 and also makes addressing of the cores quiet simple during routing. The local interconnection between the resources and routers are independent of the size of network. Moreover routing in a 2-D Mesh is easy resulting in potentially small switches, high capacity, short clock cycle and overall scalability [11]. Therefore we choose the mesh topology. A mesh topology has four inputs and four outputs from/to other routers, and another input and output from! To the PE. So we design here router for the implementation of mesh topology.

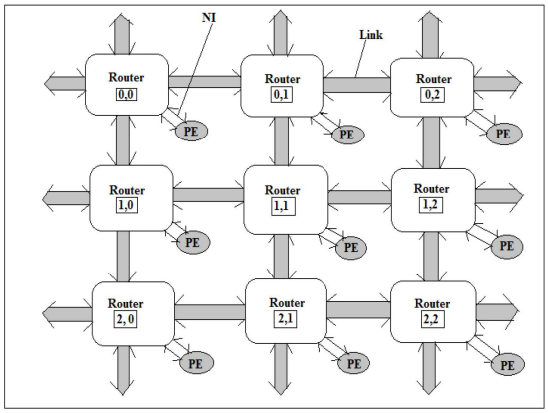


Figure 2: 3x3 Mesh topology

C. Routing Algorithm: The routing algorithm which defmes a path taken by a packet between the source and the destination is a main task in network layer design of NoC[8]. According to how a path is defined to transmit packets, routing can be classified as deterministic or adaptive. In deterministic routing, the path is uniquely defined by the source and target addresses. Deterministic routing algorithms are widely used due to easy implementation. and in adaptive routing algorithm use information about the network's state to make routing decisions. A mesh network topology consists of m column and n rows. The routers are situated in the interconnection of two wires and processing element near routers. Addresses of routers and resources can be easily defined by X and Y coordinates in a mesh. Hence for Mesh topology XY deterministic routing algorithm is used.

## NOC ROUTER

The router is the most important component in a network on chip[8]. It is the communication backbone of a NoC system. So it should be designed with maximum efficiency. Routers are used on a network for directing the traffic from the source to the destination. It coordinates the data flow which is very crucial in communication networks. Routers are intelligent devices that receive incoming data packets, inspect their destination and figure out the best path for the data to move from source to destination. A router is built according to the OSI model of network on chip. Each layer performs its own specific functions. In Fig. 3, an NoC central router in mesh topology is shown. The central router has 5 in/out port. The local port in utilized to connect the correspondent circle to the processing element (PE) and other ports are for connecting to other routers[9].

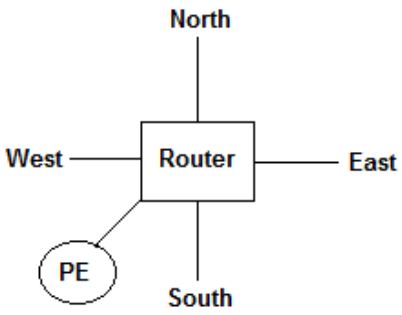


Fig. 3. A central NoC Router

## ROUTER ARCHITECTURE

Fig. 4 shows the entity of the designed router. It consists of five data input ports (datai1, datai2, datai3, datai4, datai5), five data output ports (datao1, datao2, datao3, datao4, datao5), five packet available indicators (Wr1, Wr2, Wr3, Wr4, Wr5), a clock(Clock) and a reset(Reset) signal. Fig. 5 shows the internal architecture of the designed router.

The building blocks of router consist of mainly three parts

1. Registers and demultiplexers

2. First In First Out Registers

3. Schedulers.

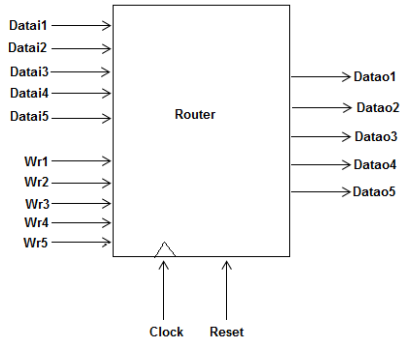


Fig. 4. The router ports

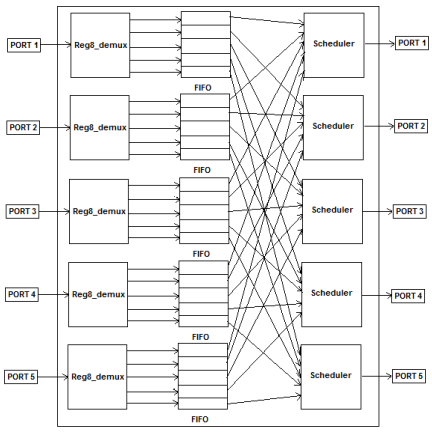


Fig. 5. The router architecture

A. Register and demultiplexer :- Fig. 6 shows the combined register and demux design. The register is used for storing the input data in the form of a buffer. The demultiplexer will direct the input to the appropriate output port.

1) 8-bit register: The register has a positive edge clock, an active high clock enable and an active high asynchronous reset. The output of the register is the input of the demultiplexer. The data input to the register is transferred to the output port at the positive edge of the clock if and only if the enable is 1

and the reset is 0. If the reset is 1, then the output port of the register is set to zeros. If the enable is 0, then the output port keeps its current value.

2) 1-to-8 8-bit demultiplexer: The demultiplexer directs the input to the proper output port according to the select signal. The select signal is taken as the first three bits of the input data. The demultiplexer also has an enable. If this enable is set to 1, then the input data is transferred to the appropriate output port and the corresponding write enable is set to 1, while the other output ports and write enables are set to zeros. If the enable signal is 0, then the output ports and the write enables are all set to zeros.

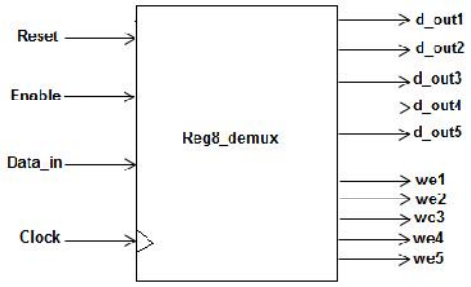


Fig. 6. Combined register and demux design

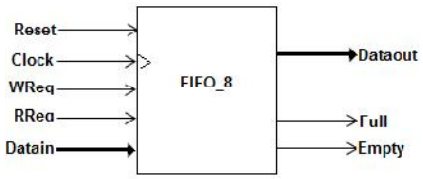


Fig. 7. FIFO Unit

B. FIFO Unit:- The FIFO unit, as shown in Fig. 7 consist of two parts RAM memory and FIFO Control. The FIFO receives read and write requests from RReq and WReq signals respectively. When the FIFO is full, write operations are disabled and when it is empty, read operations are disabled. The FIFO empty flag is set to high when the FIFO is empty and full flag is set to high when the FIFO is full.

1) RAM: The write and read operations in the memory are synchronized with the memory clock input (Clk). If (Clk) is rising and (Wr Enable) is 1, then the input data word (D in (Clk) is rising and (Rd Enable) is 1, then the output data word (D out) is read from the memory location with the address (Addr). The input bus (Datain) of the FIFO is the input bus of the RAM (D in), while the output bus (Dataout) of the FIFO is the output bus of the RAM (D out). The width of all the data ports is eight bits. When the memory is reset asynchronously by the reset signal (Rst), all its locations become zeros and its output (D out) is set to zeros as well.

2) FIFO Controller: The FIFO controller receives read and write requests from the (R Req) and (W Req) signals respectively. It checks the validity of the read or write operations and generates valid signals on (Read En) or (Write En) ports.Then it outputs the corresponding read or write address on (Add Output). The (Read En) and (Write En) ports are connected to the (Rd Enable) and (Wr Enable) ports of the RAM, respectively. The (Add Output) port is connected to the (Addr) port of the RAM.

C. Scheduler :- The scheduler used here (Fig. 8) is a round robin scheduler which uses the round robin algorithm. It assumes that all data are equally valid for selection. The algorithm lets every active data flow that has data packets in the queue to take turns in transferring packets on a shared channel in a periodically repeated order. The port through which the data comes at the present instance should have the lowest priority at the next round of scheduling. The outputs RR1, RR2, RR3, RR4 and RR5 are used to indicate the next port to be read and they are further connected to the read request ports in the corresponding FIFO.

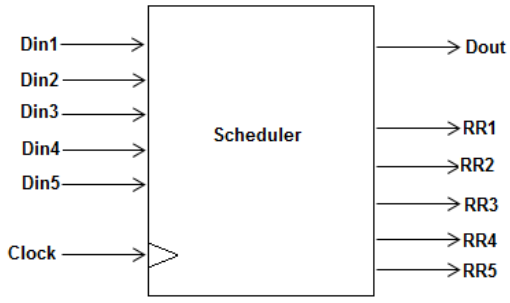


Fig. 8. Scheduler

## SIMULATION

Simulation refers to the verification of a design, its function and performance. It is the process of applying stimuli to a model over time and producing corresponding responses from a model. The simulation is performed in XILINX ISE 10.1 [10] software. A test bench is also written to test the routing pattern from various data packets. As a example Fig. 9 shows the simulation result of five port router. The reset (rst) signal must be kept low during normal operations. The write enable (wr) signals, when high, will enable the corresponding demultiplexers. The input signals (data1) are the data packets given to the router. The routing pattern is observed from the output signals (datao). The output signals

follow the round robin scheduling algorithm. The data at the input ports is directed to the output port depending on the first three bits of the input data which act as the select lines of the demultiplexer. The input data F1 from port 1 is directed towards port 1 of the output since the first three bits of the data is 1. At that instance the round robin scheduling signal of r2 will be high which indicates the port to be read in the next instance. Like wise the other data packets are also routed. From the simulation it is also observed that, depending on the amount of input data packets the router will have a delay before the output data becomes error free.

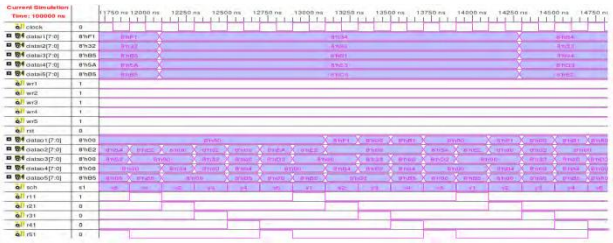

Fig. 9. Simulation result of five port router

## CONCLUSIONS AND FUTURE WORK

A five port router using simple decoding logic is proposed in this paper. The synthesis and simulation of the proposed router is verified through VHDL codes using XILINX ISE 10.1 software. The simulation facilitates clear understanding of routing pattern and the functionality of a five port router for a network on chip. In future, we intend to work on improving the scheduling algorithm used in the router for better performance.

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