Diminution of Thermal Generation of Current in Tristate Inverter Using High-Dielectrics

Manish Kumar Joshi[1], Asst. Prof. Saima Ayyub[2], Prof. Paresh Rawat[3]

Abstract: Scaling of device in CMOS which obeys Moore's law to reduce the active area of the device to its atomic dimension. High dielectric constant should be used to reduce the tunnelling effects resulting in increase of T.G.(Thermally Generated) current. In recent era of electronics high dielectric material have gained high attention.SiO_2 is widely used because it is having good manufacturing ability & high performance due to its thin size. out of various high dielectric materials recently $LaAlO_3$() have gained high attention in the field of Electronics, due to its various features such as high band gap, high dielectric constants & can resist high temperature.

Keywords: High k, Tri State Inverter, Low Power, CMOS.

1.INTRODUCTION

Regular development to CMOS processing had given birth to a technical challenge to the silicon industry because of its restriction to SiO_2 gate dielectric layer. For the performance improvement of MOS transistors the manufacturing companies shrinked the thickness of gate dielectric to 1.20 nm which increased the transistor speed but due to thin layer of SiO_2 leakage of current occurred this leakage current is also called Thermally generated current or Reverse current, resulting energy (heat) wastage. High dielectric materials should be used to prevent the tunnelling effect.

This Work gives get rid of problems like:

1. Minimise thermally Generated Current.
2. Increase the efficiency and the performance of tri state inverter.

The work based on different high dielectric material named Silicon di oxide, Silicon nitride, Aluminium Oxide, Tantalum Penta Oxide, Hafnium Oxide and Lanthanum Oxide and Different Semiconductor like Germanium, Gallium Arsenide, Silicon.

Requirement of High Dielectric Applications are as:

1. Large Band Offset with the Electrode.
2. Large Energy Band Gap.
3. High Dielectric Constant Value.
4. It Should be compatible with the gate electrode material.
5. High Break down value of voltage and good reliability.
6. It should also be Thermally and Chemically stable with semiconductor substrate.

For the purpose of Mathematical analysis we first design the Tri State Inverter on Microwind for finding out width and length for different combination of Dielectric material then do a brief study of the property of materials Such as

- Energy Band Gap.
- High dielectric Constant.
- Length in Microns
- Electron Mobility.
- Hole Mobility.

Table 1 Comparison Of property of Semiconductor material

Property	GaAs	Si	Ge
Dielectric constant	13.1	11.9	16
Intrinsic carrier con.	2.4 $\times 10^{13}$	1.45 $\times 10^{10}$	1.79 $\times 10^{6}$
Electron Mobility	8500	1500	3900
Hole Mobility	400	450	1900
Energy Band Gap ev	1.4	1.2	0.66
Atomic Weight	144.63	28.09	72.6
Crystal Structure	Diamond	Diamond	Diamond
Lattice Constant	5.5	5.4	5.6
Melting Point	1238	1415	937

Then we will find which one is effective.

A Brief Comparision in between Gallium Arsenide(GaAs) and Silicon (Si) They Both Requires Lithographic Process but there are some advantages of GaAs over Si:

- With Respect to Silicon, GaAs has high Electron mobility.

- Higher Opto-electrical properties.
- GaAs has good factor of 1.40 for carrier saturation velocity as compared to silicon.
- Less Power dissipation than silicon.

With the help of a comparision table we can better understand the electronic and physical properties of GaAs, Si and Ge.

2. LITERATURE REVIEW

D Nirmal,P Vijay Kumar, "Nanoscale Tri Gate MOSFET for Ultra Low power applications Using High-K Dielectrics", Nanoelectronics Conference (INEC), IEEE 5 thInternational. 2013.

This is our base paper in this paper d-nirmal tries to explain that complementary metal oxide semiconductor technique gives high and improved performance which can be achieved through the use of high quality material, improved design, and process innovations. The sio2 gate dielectric is changed by various high dielectric constant materials and simulation has been observed. From here it can be concluded that the thermally generated current of the circulatory is minimized by about 55%.

D Nirmal,P Vijay Kumar, "Nanoscale Channel Engineered Double Gate MOSFET for Mixed Region", International Journal of Circuit Theory and Application, 10 Mar 2012.

in this paper we have seen that the effect of gate on ID-V_{gs} properties, for different high di-electric constants using T-CAD ISE. Trans conductance of dual material gets doubled. We can reached to the conclusion that drain current increased by 5% in sub threshold region and when it is in trans conducting region it is increased by 3%.

Chih-Ting Yeh "Power-Rail ESD Clamp Circuit with Ultralow Standby Leakage

Current and High AreaEfficiency in Nanometer CMOS Technology"IEEE

Transactions On Electron Devices, Vol. 59, No. 10, October 2012.

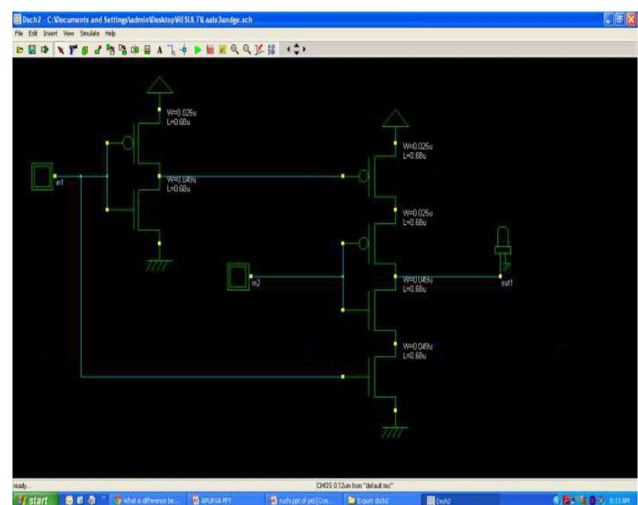
In this Paper to produce ultra low thermally generated current and efficiency of its area has been verified in 65-nm fully silicate complete mentary metal oxide semiconductor technique with the help of new designed power rail ESD clamp devise. It realised that by only 1-V devise, ESD detention device works without suffering the reverse current issue. It has been measured that the thermally generated current was 16.46 n-amp under 1-V at 25degree centigrade.

J.Conde,A. Cerdeira et al,"3D Simulation of Triple Gate MOSFET with Different Mobility Region", Microelectronics engineering Vol 88, Issue 7,pp.1633-163,July 2011

This paper gives us new idea to analyse the 3-dimensional structure of tri gate MOSFET having 3 different mesh regions. The structure is as follows: 1 ,esh region is at the top & remaining two mesh regions lies in the fin's side walls. It allows us to consider different mobility carrier at each region, because of its technological processing and fine crystalline orientation. In each region a method is developed to extract the mobility parameter of device. proposed methodology, made for fin FET array's obtained a good results between simulated value and experimental output. When arrays are taken at different fin width and at fixed channel length.

3.TRI-STATE INVERTER

One p-MOS and One n-MOS transistor are used for designing a CMOS inverter. 0 and 1 are the only two logical symbols, when several inverter share a particular node (bus structure), problem will arise hence to avoid multiple access at the same time tri-state inverter are used ,featuring the possibility to remain in a "high impedance" state when access is not necessary. It consist of an enable control circuit and a logic inverter as long as the enable En is set to its lower value (0) the output remains in high impedance.



Ordinary complementary metal oxide semiconductor inverter is not connected directly to $V_{dd\ and}$ V_{ss} supply. Whenever the cell is disabled, p MOS and n MOS devices are inserted for disconnecting inverter.

Table 3. Truth Table for Tri State Inverter.

In	En	Out
0	0	X
0	1	1
1	0	X
1	1	0

When En =1 (enable is 1) the cell works as Regular inverter (CMOS Inverter) , but when En=0 (Enable is 0) the outcome is unpredictable in nature or it 'floats' and generates fluctuation at input also generate leakage.

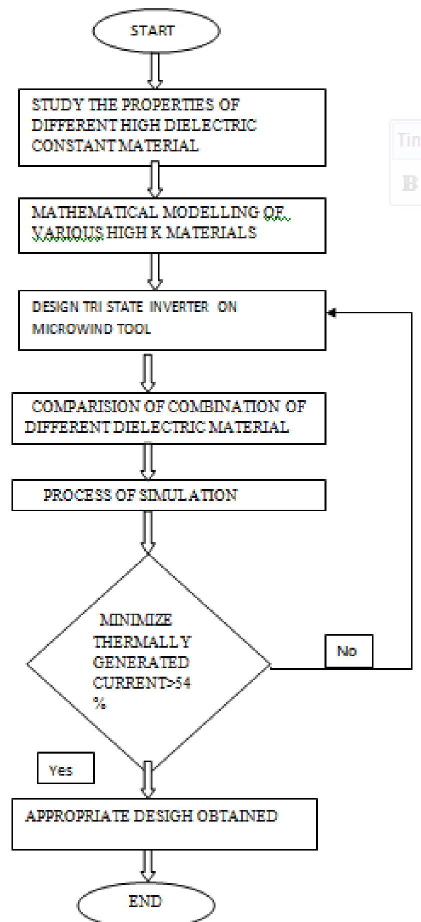
The main sources for generation of thermally generated current are:

1.Drain/Source junction thermally generated current.

2.Thermally generated current due to Direct gate tunnelling.

3.By the channel of an OFF transistor sub threshold leakage occurs.

4.PROPOSED METHODOLOGY



5.CONCLUSION

In the paper, Various high dielectric material explored on three state inverter and Different combination of Semiconductor material and oxides have been used. The output of the structure drawn and simulation process done by Microwind tool. Various oxides like silicon dioxide, Aluminium Oxide, Silicon Nitride, Hafnium Oxide, Tanalum Oxide, Lanthanum Oxide are used. Three semiconductor materials named Silicon, Germanium and Gallium Arsenide also used. Our requirement is to analyse mathematically the value of thermally generated current on tri state inverter and then for all possible combination semiconductor and oxide we compare the resultant and then conclude which material gives lower value of thermally generated current.

REFERENCES

[1] D Nirmal,P Vijay Kumar, "Nanoscale Tri Gate MOSFET for Ultra Low power applications Using High-K Dielectrics", Nanoelectronics Conference (INEC), IEEE 5thInternational. 2013.

[2] Nirmal 1,divyamarythomas 3,Shruti.k 4 and patrickchellaSamuel" Impact of Gate Engineering on Double Gate MOSFET using High-k Dielectrics"IEEE 2011.

[3] J.Conde,A. Cerdeira et al,"3D Simulation of Triple Gate MOSFET with Different Mobility Region", Microelectronics engineering Vol 88, Issue 7,pp.1633-163,July 2011.

[4] X. Zhou, "Exploring the novel characteristics of hetero-material gatefield-effect transistors (HMGFETs) with gate-material engineering," IEEE Trans. Electron Devices, Vol. 47,2000.

[5] A. P. Huang1,2, Z. C. Yang1 and Paul K. Chu2, "Hafnium-based High-k Gate Dielectrics, " Advances in Solid State Circuit Technology.

[6] N.Mohankumar, BinitSyamal, and Chandan Kumar Sarkar, "Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs," IEEE Transactions On Electronic Devices, Vol. 57.

[7] Integrated Systems Engineering (ISE) TCAD Manuals, Integr.Syst.Eng., Zurich, Switzerland, 2006. Release 10.0.33,

[8] J. Yuan and J. C. S.Woo, "A novel split-gate MOSFET design realized by a fully silicided gate process for the improvement of transconductance and output resistance," IEEE Electron Device Lett.,vol. 26, 2005.

[9] Chih-Ting Yeh "Power-Rail ESD Clamp Circuit with Ultralow Standby Leakage Current and High Area Efficiency in Nanometer CMOS Technology" IEEE Transactions On Electron Devices, Vol. 59, No. 10 october 2012.

[10] J. P. Colinge, "Multiple-gate SOI MOSFETs," Solid State Electron.,Vol. 48, 2004.