A Linear Phase Detector Circuit Using OTRA

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Abstract* - *In this paper, an Operational Trans-Resistance Amplifier (OTRA) based Phase Detector circuit has been proposed. The circuit is simple to realize and have a low component count. SPICE simulations have been given to verify the theoretical analysis

Keywords – OTRA, PD, CMOS, VCO, CDR.

1. INTRODUCTION

The clock and data recovery (CDR) circuit is an integral part of high-speed serial data communication systems and phase detectors play an essential role in CDR circuits [1]. Extensive literature review suggests that the existing phase detector circuit design approaches can broadly be classified as those based on (1) Digital techniques [2-5] and (2) Analog Techniques [6-7]. It produces an output voltage proportional to the input phase difference. The main advantage of using OTRA is that being a current-mode device, the bandwidth of OTRA is independent of the closed loop gain. In addition, it is free from parasitic input capacitances and resistances, as its input terminals are internally grounded.

The paper is organized as follows: Description of OTRA is presented in Section II. Section III introduces the proposed phase detector. Section IV describes the simulation results of the circuit and finally Section V concludes the paper.

OTRA: The circuit symbol of the OTRA is illustrated in Fig. 1. The port relations of an OTRA [9] can be characterized by the following matrix equation.

$$\begin{bmatrix} V_p \\ V_n \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_z \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

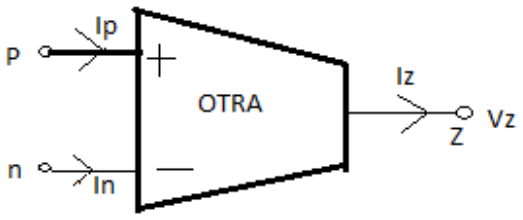


Figure 1: Symbol of the OTRA with its matrix

The input and output terminals of the OTRA are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are internally grounded leading to circuits that are insensitive to the stray capacitances. For ideal operation, the trans-resistance gain (R_m) approaches infinity forcing the input currents to be equal. Thus, the OTRA must be used in a negative feedback configuration [8-11].

2. SYSTEM MODEL

The block diagram of a phase detector is shown in Fig 2. The phase detector is a 3-port configuration. A sinusoidal signal Vc = cosωt is applied as a reference signal to input port 1 of the phase detector. When a phase coherent signal *Vs = Cos(ωt-Φ)* with a carrier frequency of *ω* and an instantaneous phase deviation (*Φ)* is applied to input port 2 of the network, a response signal *V(Φ),* proportional to the phase deviation (*Φ)* would be obtained from the output Port 3 [6-7].

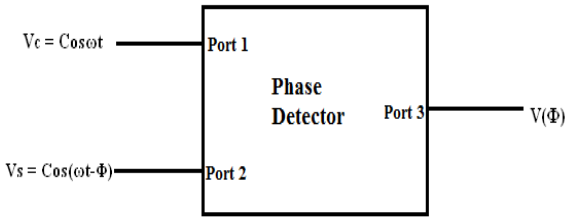


Fig.2. Phase Detector block diagram

The architecture of the proposed phase detector is shown in Fig. 3. It consists of 2 OTRAs, a CMOS XOR circuit and an RC integrator. To interface the XOR gate with the integrator, a buffer circuit is used so that the loading effect of the integrator can be avoided. Both the OTRAs are used in open loop configuration to work as comparator. A sinusoidal signal without any phase deviation is applied to comparator 1 as a reference signal. The sinusoidal signal whose phase is to be detected is applied to comparator 2.

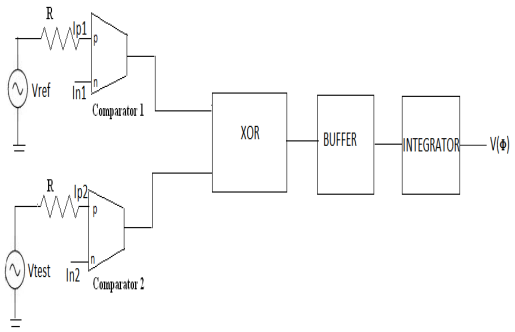


Fig.3.Proposed phase Detector circuit

3. PROPOSED METHODOLOGY

The logical operation of the proposed phase detector is as follows:-

A sinusoidal signal v(t) = A Cosωt of time- period T is applied to p terminal of the OTRA comparator. For positive amplitude of v(t), the output of the comparator is a rectangular pulse of amplitude A. For negative amplitude of v(t), the output of the comparator is zero. When a sinusoidal signal with time-period T and delay in phase Φ represented by $v_1(t)$ = A Cos$(\omega t - \Phi)$ is applied to the comparator, the output of $v_1(t)$ is same as the above mentioned rectangular pulse but delayed in time by Φ/ω . Fig. 4(a) and Fig. 4(b) shows the output waveforms of comparator for v(t) and $v_1(t)$ respectively.

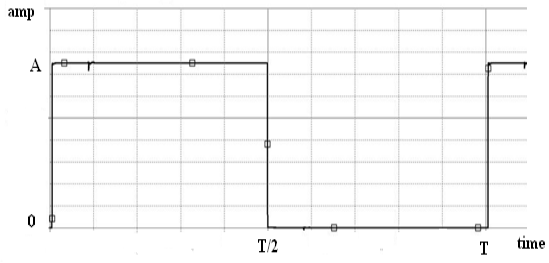


Fig. 4(a): Output of comparator for v(t)

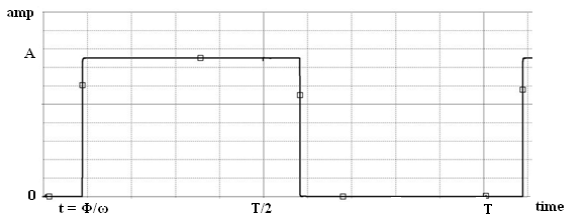
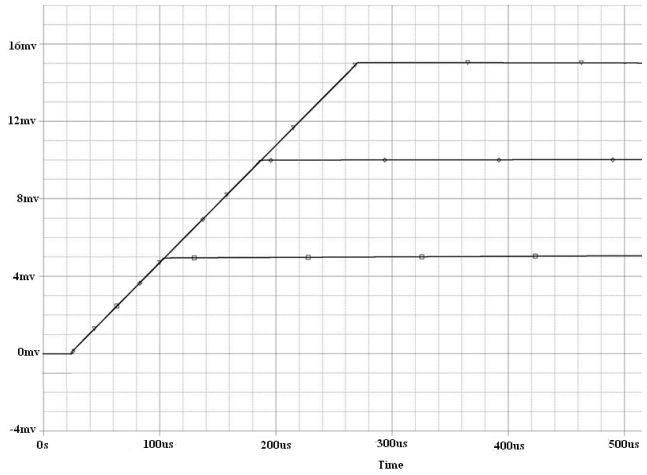


Fig. 4(b): Output of comparator for $v_1(t)$

These two outputs of the comparator are applied as the two inputs to a XOR gate. For simplicity, the output of the XOR gate for half of the time-period is considered. The output of the XOR gate will be high from t =0 to t = Φ/ω and from t = Φ/ω to t =T/2, the output will be low. The output of the XOR gate is integrated from t =0 to t =T/2 to obtain a voltage V(Φ) called output voltage of the phase detector. It can be observed that V(Φ) directly depends on the time t = Φ/ω which is time delay in the output of the comparator for input signal $v_1(t)$. So, more this delay, more is the value of V(Φ). As t = Φ/ω is proportional to Φ, so V(Φ) is proportional to Φ.

For detecting a phase-delay (Φ) present in any sinusoidal signal V_c =Cos$(\omega t - \Phi)$, a reference voltage Vref = cosωt of zero phase delay is applied to comparator 1 while V_c = Cos$(\omega t - \Phi)$ is applied to comparator 2. The output of the integrator, V(Φ) is proportional to the phase delay (Φ) which can be calculated by simple algebraic calculation.

4. SIMULATION/EXPERIMENTAL RESULTS



5. CONCLUSION

In this paper, an Operational Trans-Resistance Amplifier (OTRA) based Phase Detector circuit has been presented. All the components except the buffer has been composed of active elements .In future, this component may be replaced by any other active-element circuit which would reduce the power requirement of the proposed phase detector circuit .The theoretical results have been presented by SPICE simulations result.

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