# Literature Review on WiMAX Physical Layer Optimization

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***Abstract-The Viterbi algorithm (VA) is a popular method of decoding convolutional codes for its fairly low hardware complexity and relatively good performance. Soft-Output Viterbi Algorithm (SOVA) proposed by J. Hagenauer that is a modified Viterbi Algorithm. A SOVA decoder can not only take in soft quantized samples but also provide soft outputs by estimating the reliability of the individual symbol decisions. These reliabilities can be provided to the subsequent decoder to improve the decoding performance of the concatenated decoder. The SOVA decoder is designed to decode the convolutional codes defined in the ECMA-368 standard. Its code rate and constraint length is R=1/3 and K=7 respectively. To speed up the add-compare-select unit, that is always the speed bottleneck of the decoder. In the SOVA decoder, the delay line storing the path metric difference of every state contains the major portion of the overall required memory. A novel hybrid survivor path management architecture using the modified trace-forward method is proposed. It can reduce the overall required memory and achieve high throughput without consuming much power.***

***Keywords: - WiMAX, Decoding Algorithms, SISO; Shannon limit and Viterbi algorithm.***

## I. INTRODUCTION

In recent years, there is an increasing need for high-throughput high-performance digital wireless communication and the relative technology is developed rapidly to meet our need. In terms of mobile communication, the third generation mobile communication system such as WCDMA, CDMA2000 and TD-SCDMA have been brought into commercial operation in many countries including China. And its successive version, the third generation long term evaluation (3G-LTE), is under research and supposed to be used in the recent future. The third generation mobile communication system can reach a data rate of dozens of Megabits per second (Mbps) in its downlink and 3G-LTE mobile communication system is designed to reach up to several hundred Mbps in its downlink! On the other hand, for the short range digital wireless communication system, the ultra wide band (UWB) wireless communication technology, which can transfer data at a speed over 100 Mbps within 10 meters, has been studied for several years worldwide. It is supposed to be used in physical layer of the wireless personal area network (WPAN) and next generation Blue Tooth. Multiband Orthogonal Frequency Division Modulation (MB-OFDM) is a very popular scheme to implement the UWB system and is adopted as the ECMA-368 standard [1]. And China is going to publish its own UWB standard in the recent future. Fig. 1 shows the evaluation roadmap of wireless communication system.

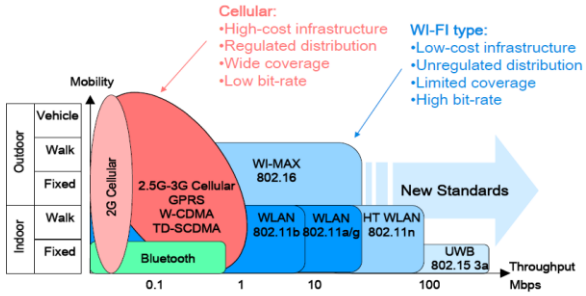


Fig.1. Evaluation of wireless communication systems

When data are transferred between transmitter and receiver in wireless communication system, they are easily to be interfered by the channel which will bring noise to the data and attenuate them as well. To make the high speed data transferred over the channel reappear reliably at the receiver, the error correcting encoder and decoder, which can generate error correcting codes (ECC) and decoding the codes respectively, must be utilized. The error correcting encoder and decoder are also usually called channel encoder and decoder. Fig. 2 is a block diagram which shows how the channel encoder and decoder can be used in the digital communication system.

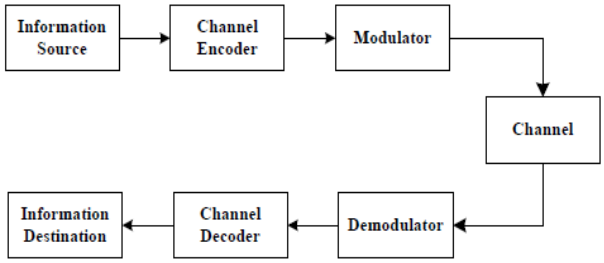


Fig.2. A typical communication system

*Convolutional Code and Convolutional Encoder*

Convolutional code can be described by three integers: *k*, *n* and *K*. The ratio *k* / *n* is the rate of the code and *K* is called the constraint length of the code. The output of a convolutional encoder depends not only on the current input information,but also on the previous inputs. That means the convolutional encoder is a sequential circuit or a finite-state

machine. In fact, a convolutional encoder can easily be constructed by some registers and XOR gates. All the registers form a shift register and the number of these register plus one is the constraint length.

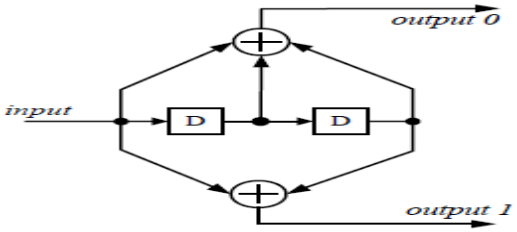


Fig.3. A simple convolutional encoder

In practice, the next state of the convolutional encoder can be predicted if its current state is known. For example, if the current state is 01(it means the content of the left register is 0 and the content of the right register is 1), the next state will be 10 is the current input is one and will be 00 if the current input is zero. So a table which lists all possible current states and their corresponding next states and outputs can be constructed, as Table 2-1 shows. i S 1 i S

| Current state | Current input | Next state | Current output |
|---|---|---|---|
| 00 | 0 | 00 | 00 |
| | 1 | 10 | 11 |
| 01 | 0 | 00 | 11 |
| | 1 | 10 | 00 |
| 10 | 0 | 01 | 10 |
| | 1 | 11 | 01 |
| 11 | 0 | 01 | 01 |
| | 1 | 11 | 10 |

Table 1 table describe the convolutional encoder

## II. SYSTEM MODULE

*Viterbi Decoding Algorithm*

The Viterbi algorithm is a very common and efficient method to decode the convolutional codes. It is a maximum likelihood decoding algorithm in the sense that it finds the closest coded sequence to the received sequence by processing the sequences on an information bit-by-bit basis. It is more convenient than the "brute force" decoding strategy mentioned above because it reduces the computational complexity by taking advantage of the special structure in the trellis diagram [13].

When two paths enter the same state, Viterbi decoder (that is, a decoder using Viterbi algorithm to decode the convolutional codes) selects the one with better metric and discards the other path. The path selected is called the survivor path. By repeating this operation for every state and at every time, the Viterbi decoder can remove from consideration those trellis paths that could not possible be the maximum likelihood before the final comparison is done. The early rejection of the unlikely paths reduces the decoding complexity. To describe the Viterbi Algorithm in detail, an example of Viterbi decoding procedure is introduced below. In this example, assume is the channel is BSC. The encoder is shown in Fig. 4 and the corresponding trellis is shown in Fig. 5. Assume that the message sequence to be encoded is 01011100101000100 (The last two zero bits are used to make the encoder return to all-zero state), it can get the encoder's output sequence, which is:

00 11 10 00 01 10 01 11 11 10 00 10 11 00 11 10 11

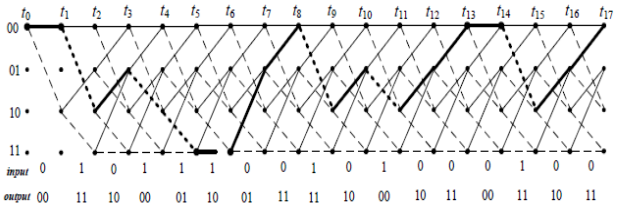


Fig.4. Encoding process

At time 1 *t*, the received symbols is 00. Therefore, the branch metric from state 00 at time 0 *t* to state 00 at time 1 *t* is 0 and the branch metric from state 00 at time 0 *t* to state 10 at time 1 *t* is 2. Since the previous accumulated metric are both 0, the accumulated metric for state 00 and state 10 at time 1 *t* is 0 and 2 respectively. The accumulated metric of every path is also called path metric and the accumulated metric of every state is called state metric. If there is only one path merging at one state, its state metric is the metric of the path. Fig. 5 shows the decoding operation at time 1 *t*.

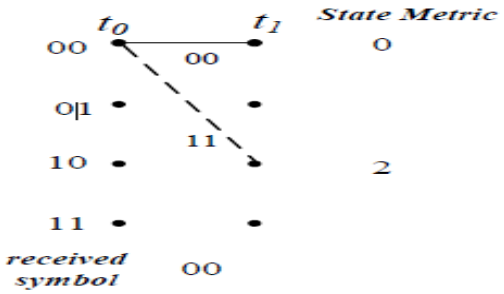


Fig.5. Viterbi decoding operation at 1 *t*

*The SOVA Turbo Decoder*

Turbo decoder extracts the systematic bits and recursive bits from the received information. A basic block diagram of turbo decoding process is shown in figure. The input to the turbo decoder is the received sequence represented as $R_k = [Y_{sk}, Y_{pk}]$ it consists of two decoders DEC1and DEC2. DEC1 decodes sequence from ENC1 while DEC2 decodes sequence from ENC2. Each of the decoder acting as Maximum A Posteriori (MAP) decoder.

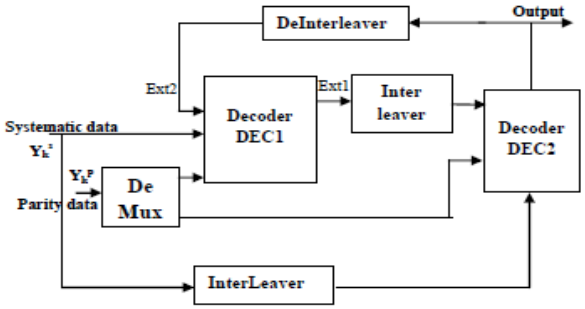


Fig.6. Structure of Turbo decoder

*Soft Output Viterbi Algorithm*

The Viterbi algorithm (VA) is a widely-used method for maximum likelihood decoding, and its simple architecture makes it an easy choice in most practical applications. One of its shortcomings, however, is its inability to provide soft-decision


Fig.7. Block diagram of the soft output Viterbi algorithm

## III. LITERATURE REVIEW

In the year of 2015 Nguyen, C.D.; Jaejin Lee,[1] Investigated a new detection scheme using three extrinsic information resources supporting two-dimensional soft output Viterbi algorithm (2D SOVA) for bit patterned media recording (BPMR) that is well-known as a candidate for the next-generation magnetic storage system. The presented method allows channel detection to improve its output with the help of the useful extrinsic information resources in each stage.

In the year of 2014 Kene, J.D.; Kulat, K.D.,[2] presented relatively better performance as compare to convolution codes at lower Signal to Noise Ratio. Turbo code offers an outstanding coding gain very close to Shannon limit over an AWGN channel to achieve maximum throughput particularly for WiMAX application. The objective of this research work is to Study the Mobile WiMAX system performance by implementing the turbo codes using Soft Output Viterbi Algorithm (SOVA). Turbo decoder is optimized by modifying the SOVA that contributed to the system performance optimization. For different transmission conditions, BER performance has been simulated and compared to the conventional Log-MAP decoding algorithm. The performance of mobile WiMAX system has also been tested for the effect of various Decoding algorithms, Frame size and Code rates.

In the year of 2014 Viraktamath, S.V.; Kotihal, A.; Attimarad, G.V.,[3] presented a Classical Viterbi algorithm and Soft Output Viterbi Algorithms are used for error correction in many applications. In this research work the performance of hard decision as well as soft decision output Viterbi algorithms have been analyzed for the image transmission application. The code rate considered is ½. The performance study is done by varying the constraint lengths as well as generator polynomials. The reconstructed image gives the visual impact for the different constraint lengths, generator polynomials as well as for the different algorithms. The mean square error between the original image and the reconstructed image is also tabulated. The modulation technique used in the simulation is DPSK.

In the year of 2014 Chaikalis, C.; Liolios, C.; Vlachos, V.,[4] proposed a study of SOVA and log-MAP turbo decoding algorithms share common operations. Their analysis shows that the improved reconfigurable SOVA/log-MAP turbo decoder can be implemented in LTE systems for AWGN channel. Authors examine two data rates, and for each one author consider the nine possible QCIs using five frames. Considering BER and latency limitations for each QCI, SOVA is proposed for most of the cases for low data rates, whereas log-MAP is proposed for higher data rates.

In the year of 2012 Yue Ling; Yang Xiao-liang; Wang Ming-zhou; Fan Shu-hong, [6] presented he study of concerned with the performance of turbo coded FH/MFSK system in adverse shallow water acoustic channel. A soft decision statistic extraction algorithm suitable for noncoherent orthogonal M-ary FSK demodulation is presented. Then the system's bit error probability performance with SOVA and Log-MAP decoding algorithm is carefully investigated through computer simulations and lake trials. Both simulations and analyses of lake trials demonstrate the excellent performance of this integrated approach to reliable acoustic communications.

In the year of 2012 Lohr, M.B.; Dennis, M.L.; Funk, K.B.; Pavek, R.E.; Sova, R.M.,[7] Investigated a Concept feasibility of a photonics-enabled Ka-band subscale “radar” is demonstrated for ranging. Experimental outcomes using a corner cube reflector and stretch processing are presented, with a 28-GHz carrier modulated by 40-ns, 4-GHz chirp pulses.

In the year of 2012 Sova, D.; Radhakrishnan, C.; Jenkins, W.K.; Salvia, A.D.,[8] proposed a Fault Tolerant Adaptive Filters (FTAFs) rely on inherent learning capabilities of the adaptive process to compensate for transient (soft) or permanent (hard) errors in hardware system. This research investigates fault tolerant transform domain adaptive noise canceling filters to cancel noise from corrupted speech signals. Two transform domain adaptive FIR architectures are compared, one based on the conventional FFT and one on the Modified Discrete Fourier Transform (MDFT), both without zero padding. Outcomes support the fact that the MDFT- based FTAF architecture is able to overcome certain fault conditions that cannot be properly handled with a conventional FFT-based FTAF architecture.

## IV. PROBLEM FORMULATION

The problem Originally, Both of the decoding blocks controlled in an SCCC decoder employ the soft output Viterbi algorithm. Though much testing of this algorithm has been performed in software on general purpose processors, there is a need for a SOVA decoder circuit design which can be used throughout the remainder of the HFEC An exhaustive decoding algorithm would compare the received data with every possible path along the trellis and output the one that is most likely, but that is not feasible in most cases. The Viterbi algorithm keeps track of only the paths that occur with maximum likelihood (ML). The work presented in this research work focuses on an initial design for a SOVA decoder. The attractiveness of SOVA decoder enables us to

find a way to deliver its soft output to the RS decoder. To convert bit reliability into symbol reliability because the soft output of SOVA decoder is the bit-oriented while the reliability per byte is required by the RS decoder. But no optimum transformation strategy exists because the SOVA output is correlated.

## V. CONCLUSIONS & FUTURE SCOPE

This research work provides an easy to analysis to concatenate the SOVA decoder and RS decoder under various kinds of convolutional code rates. The scheme uses a property of the RS decoder, Data also suggest that for each B>8, the increase in BER performance becomes smaller and smaller, until it aligns with the software reference decoder. Since B = 8 is a very common bit width, it becomes a clear choice for use in most applications. It can be assumed, however, that increasing the bit width to B = 16 will provide even more accuracy, while at the same time following the standards of most hardware systems. Research work would be done to improve upon the speed and size of the structures contained in the design. One example is the current method of overflow prevention. It may be possible to remove this in the adder/subtractor circuits, while calculating the bit widths necessary to widen their inputs and outputs to accommodate all possible values. Such a change may allow for a decrease in the error encountered by restricting the range of all integers that go through an adder/subtractor, while providing a small boost in clock speed.

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