A Mux Based Low Power Full Subtractor Circuit

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Abstract

A low-power full subtractor design is proposed in this paper to minimize the active leakage power in nano scale very large scale integration (VLSI) systems. The proposed system of a full subtractor circuit uses a three transistor x-or gate circuit to generate difference and hence it reduces area and power significantly. The borrow part of the system is implemented by using Differential Cascade Voltage Switch Logic (DCVSL) multiplexer to achieve lesser power consumption over a range of power supply voltages. All the simulations can be carried out by using Tanner EDA tool, Microwind and LT Spice. In proposed method the percentage reduction obtained in power is 62%, in area is 34.65% and percentage reduction in noise is 50.4% compared to the existing MTCMOS technology.

Keywords

CMOS Circuit, Full Subtractor, Low Power Design, Leakage Current, Differential Cascade Voltage SwitchLogic(DCVSL)

1. Introduction

In the past, the major concerns of VLSI designers were performance and miniaturization. With the substantial growth in portable computing and wireless communication in the last few years, power dissipation has become a critical issue. Problems with heat removal and cooling are worsening because the magnitude of power dissipated per unit area is growing with scaling. Years ago, portable battery-powered applications were characterized by low computational requirement. Nowadays, these applications require the computational performance similar to as non-portable ones. It is important to extend the battery life as much as possible. For these reasons power dissipation becomes a challenge for circuit designers and a critical factor in the future of microelectronics. Power consumption in CMOS circuits can be divided into three main components: short-circuit power, switching power and static power [7].

Short-circuit power arises when a conducting path between supply and ground is formed. To avoid this rise time and fall time must be approximately equal. This can be achieved by proper sizing of pull-up and pull-down circuitry. Short-circuit power consumption is significant in dynamic circuits. Careful design is required to keep this component of power dissipation small enough to be ignored. Switching power is a result of the power consumed in charging and discharging of internal node capacitance. Static power dissipation is sum of all the leakge power dissipation which is arised due to leakage currents. Some of the leakage current is present even when the device is turned off. Static power has started to form a significant portion of the total power consumption as a result of the low threshold devices normally used in advanced DSM technologies.

The power consumption reduction in digital systems involves optimization at different design levels. This optimization includes the technology used to implement digital circuits, the logic style, the circuit architecture, and the algorithm that are being implemented.

In this paper a new full subtractor design is introducing. The main key point is to reduce the static power dissipation. The circuit uses pass transistor logic, DCVSL based multiplexer and inverters to implement the concept. By following this method both area and power can be reduced to a greater extend.

A full subtractor is a combinational circuit that performs subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage [4]. This circuit has three inputs and two outputs. A, B and C are the inputs to the full subtractor A denotes minuend, B denotes subtrahend and C denotes previous borrow respectively. The two outputs are Difference and Borrow. The truth table of the full subtractor is shown in table 1.

Table-1: Truth Table of Full Subtractor

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The simplified Boolean functions for the outputs can be deduced from the truth table. The simplified logic equations for difference and borrow are:

Difference = A ^ B ^ C

Borrow = C (A'B' + A B) + A'B

The CMOS level circuit diagram of full subtractor is shown in Fig.1 and the input and output waveforms of the full subtractor shown in Fig.2.

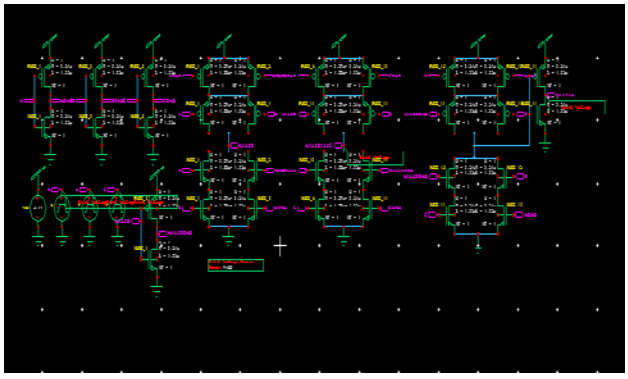

Fig.1. Circuit Diagram of a Conventional Full Subtractor.

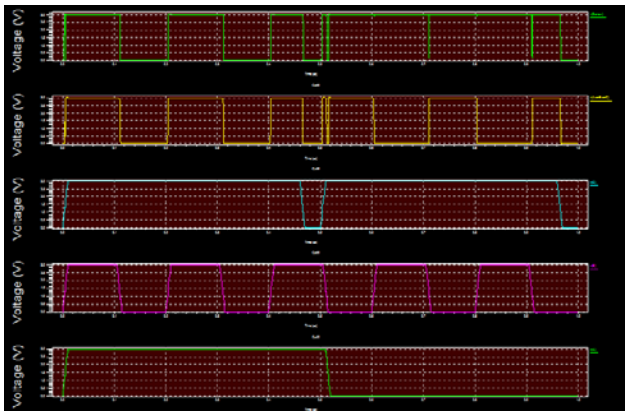

Fig.2. Waveform of Conventional Full Subtractor.

2. Existing Method

One of the popular existing low power design technique is the MTCMOS technique. MTCMOS stands for multi threshold CMOS technique. This technique uses transistrors having different threshold voltages. Generaly low, high and normal thtransistors while designing a CMOS circuit [3] [4]. When transistors are scaling down their supply voltage and threshold voltages also scale down. The reduced threshold voltage causes significant leakage current and hence increases static power dissipation. In MTCMOS technique low-threshold voltage transistors are used to implement the logic while high threshold voltage transistors are connected between supply and logic block also in between logic block and ground. Low threshold voltage transistors have high performance and hence they can be used to implement the logic in the critical path to ensure reduced propagation delay. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path .The multi threshold CMOS technology has two modes of operation. Active and sleep mode. These modes of operations are determined by sleep signal. In the active mode of operation the circuit performs its intended operation while in sleep mode it effectively cuts off the device and hence reduces leakage current significantly.

The CMOS level circuit diagram of MTCMOS full subtractor is shown in Fig.3 and the input and output waveforms of the full subtractor shown in Fig.4. The percentage power reduction in MTCMOS full subtractor compared to the conventional full subtractor is 71.35%.

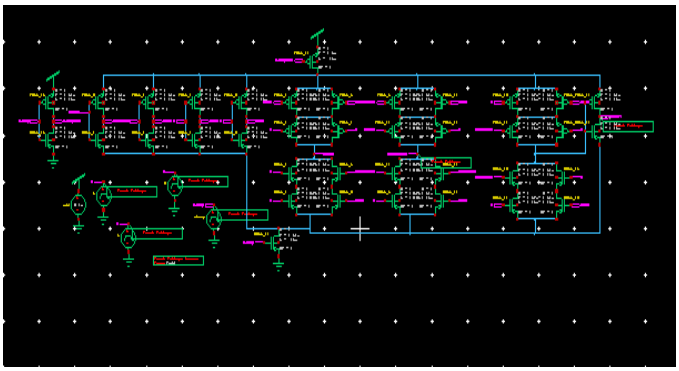

Fig.3. Circuit Diagram of MTCMOS Full Subtractor.

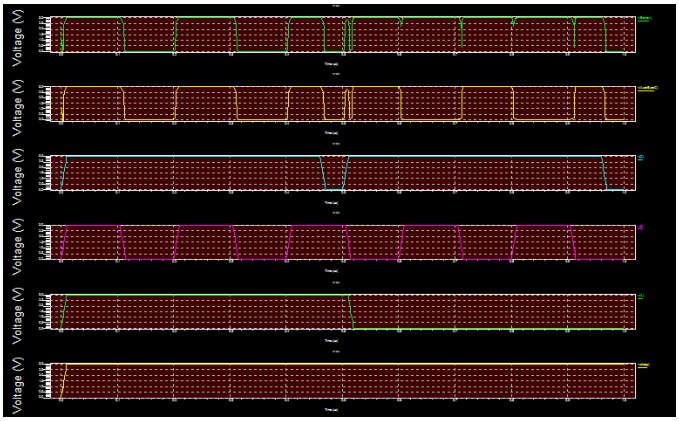

Fig.4. Waveform of MTCMOS Full Subtractor.

3. Proposed Method

A full subtractor circuit is proposing here with to reduce the area and power dissipation. A structural level optimized design of full subtractor is derived for small size circuit applications. The main building blocks of the circuit are X-OR gate, 2:1multiplexer [8] and inverters.

The 2:1 multiplexer is designed using differential cascode voltage switch logic (DCVSL) [1]. The major advantage of DCVSL technique is that a logic function and its inverse are automatically implemented in this logic style. It is a static logic and consumes no dynamic or static power. It requires true and complement inputs and it produces true and complement outputs.

A general DCVSL circuit consists of two major sections. A latch section as the upper circuit part and pulldown network block as lower section. The latch consists of two cross coupled PMOS transistors and it provides complementary outputs. The latch section allows to hold a result.

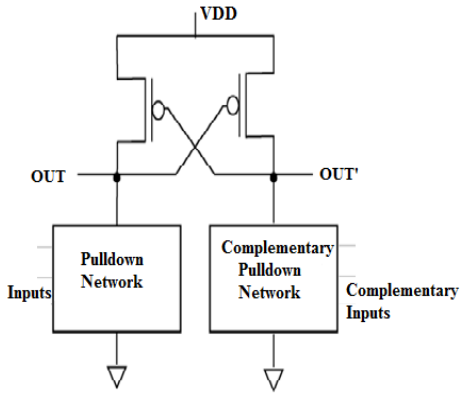

Fig.5. General Block Diagram of DCVSL Design

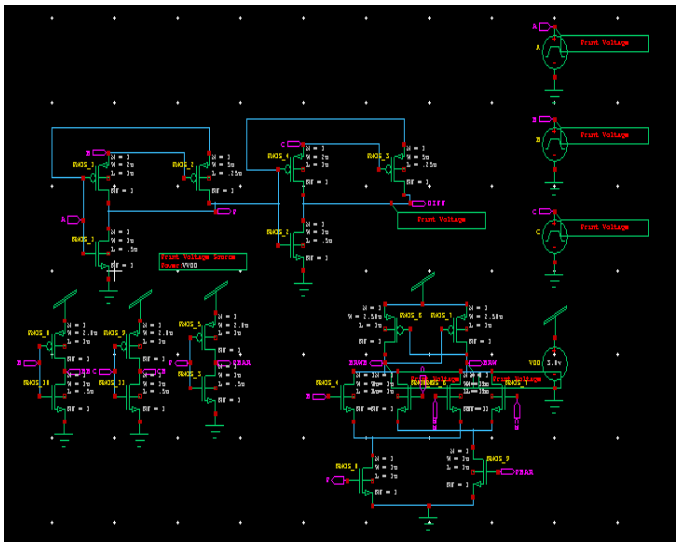

Fig.6. Circuit diagram of proposed full subtractor.

The latch is driven by pulldown network that can be viewed as two complementary switching blocks; when one block is a closed circuit (from top to bottom), the other will be in open state. Closing a switch pulls the corresponding output to ground, forcing it to logic 0 level, while the complementary output is set to a logic 1 value by latching action. The major advantage of DCVSL is in its logic density that is achieved by elimination of large PMOS transistors from each logic function [2].

The transistor level circuit diagram of the proposed full subtractor is shown in Fig.6 and the input and output waveforms of the full subtractor shown in Fig.7. The percentage reduction in power compared to the MTCMOS circuit is 62% in this design.

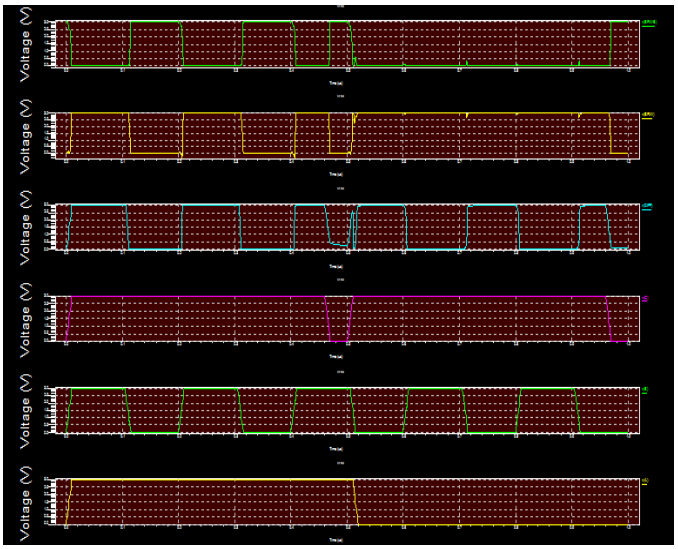

Fig.7. Waveform of proposed full subtractor.

4. Simulation Results

Transistor level full subtractor is designed using tanner tool in 35 nm technology to verify the power consumption. Fig.8, Fig.9 and Fig.10 shows the power consumption of conventional full subtarctor, MTCMOS full subtarctor and proposed multiplexer based full subtractor respectively.

Table 2 shows the comparison of conventional full subtractor, MTCMOS full subtractor and proposed full subtractor in terms of circuit parameters transistor count, area, noise and power dissipation. Circuit area and noise is compared by using microwind and LT Spice tools respectively. All the simulations are carried out in 35nm technology.

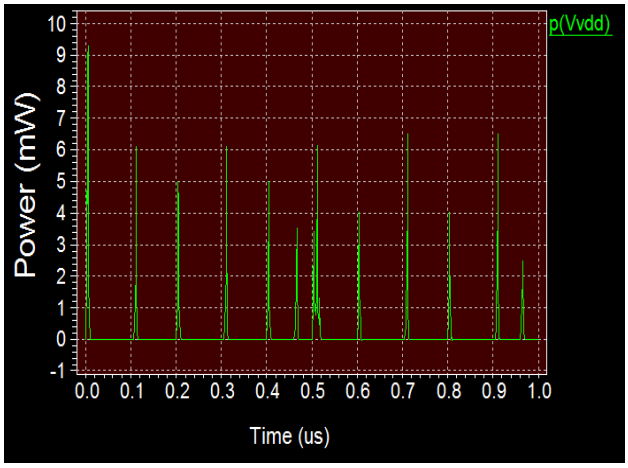

Fig.8. Power Dissipation of Conventional Full Subtractor.

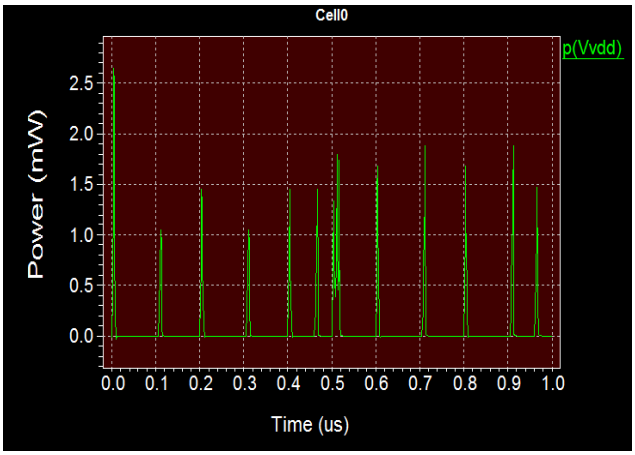

Fig.9. Power Dissipation of MTCMOS Full Subtractor.

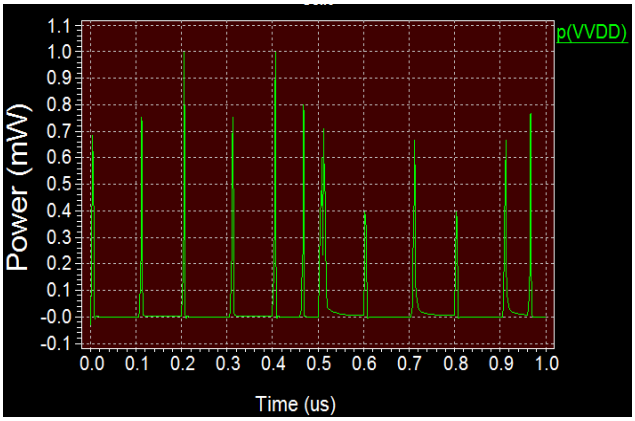

Fig. 10. Power Dissipation of Proposed Full Subtractor.

Table-2: Parameters Comparison of Various Fullsubtractors

Circuit Parameter	Circuit Structure		
	Conventional FS	MTCMOS FS	DCVSL FS
Transistor count	34	38	20
Layout area (μm^2)	8553.1	11857.9	7499.5
Power dissipation (mW)	9.25	2.65	1
Noise (pV)	17.52	33.89	16.782

5. Conclusion

A new design of full subtractor circuit has setup using pass transistor logic, cmos logic and DCVSL logic. The new design ensures considerable reduction in area, power and noise. The tools used are Tanner EDA tool,Microwind and LTSpice to findout power dissipation,layout area and noise respectively. All the simulations are carried out in 35nm technology. In proposed method the percentage reduction obtained in power is 62%, in area is 34.65% and percentage reduction in noise is 50.4% compared to the existing system.

6. Future Scopes

The proposed technique is well suitable for area and power efficient applications. The power can be further reduced by using MTCMOS technique to this design. Since the DCVSL technique gives the complementary borrow output the circuit is well suitable to implement ripple borrow subtractor.

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